NM25Q16A Datasheet

3.3V 16Mbit Serial Flash Memory with Standard, Dual and Quad SPI

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1. Features

- **16Mbit SPI NOR Flash**
  - Totally 2048K bytes
  - 256-byte Page Program
  - 4KB Sector/32KB Block/64KB Block/Chip Erase
- **Protocols Supported**
  - Standard SPI: SCLK, CS#, SI, SO, WP#, HOLD#
  - Dual SPI: SCLK, CS#, IO0, IO1, WP#, HOLD#
  - Quad SPI: SCLK, CS#, IO0, IO1, IO2, IO3
- **Single Supply Voltage**
  - Full voltage range: 2.7~3.6V
- **High Performance**
  - 120MHz maximum clock frequency
  - Dual I/O data throughput up to 240Mbit/s
  - Quad I/O data throughput up to 480Mbit/s
  - Page Program: 0.45ms typical
  - Sector Erase: 50ms typical
  - 32KB Block Erase: 120ms typical
  - 64KB Block Erase: 150ms typical
  - Chip Erase: 8s typical

- **Software and Hardware Write Protection**
  - Protection of portion or all of memory space
  - Protection enabled/disabled by WP#
  - Top/Bottom protection mechanisms
- **Low Power Consumption**
  - 10uA Standby current
  - Maximum 20mA active current
  - Typical 1uA power down current
- **Advanced Security Features**
  - 3*1024-byte Security Registers with OTP lock
  - 128-bit Unique ID for each device
- **Temperature Range**
  - Commercial: 0℃ to +70℃
  - Industrial: -40℃ to +85℃
- Endurance of 100,000 Program/Erase Cycles
- Data Retention of 20 Years
- Industry Standard Packaging
  - SOP8, SOP16
  - DIP8
  - WSON8
  - TFBGA-24

2. General Description

The NM25Q16A is a 16Mbit Serial Peripheral Interface (SPI) NOR Flash memory device which supports standard SPI, Dual SPI and Quad SPI modes with user pins being SCLK, CS#, SI, SO, WP# and HOLD#, and the latter four of them may also function as IO0, IO1, IO2 and IO3.

The main array of the device can be viewed as a 2M-byte array of data bytes, which can be erased at a variety of granularities, programmed or written in a maximum of 256-byte pages and read for any volumes of bytes.
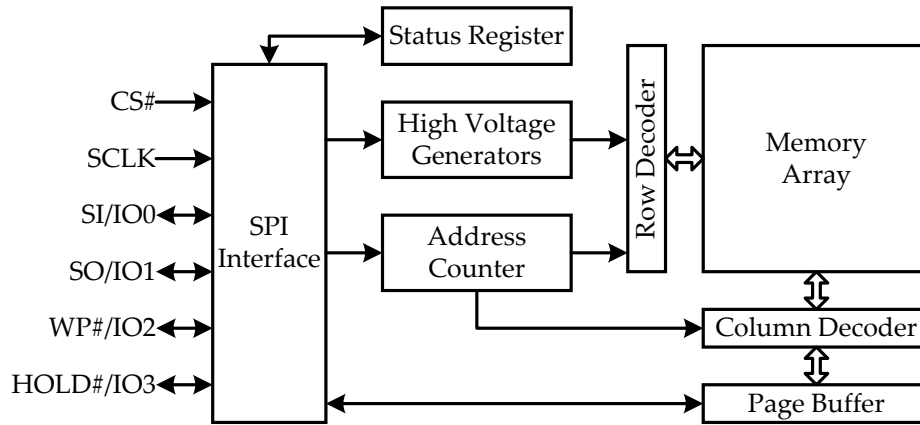
Figure 1: NM25Q16A SPI Flash Block Diagram

3. Pin Configuration

The NM25Q16A device has the following pin configurations.
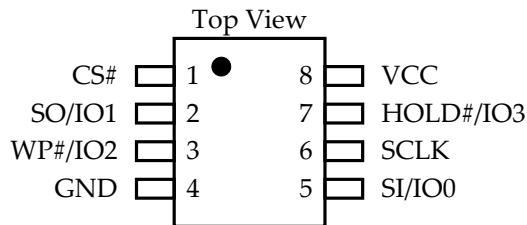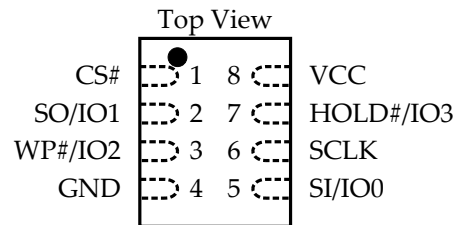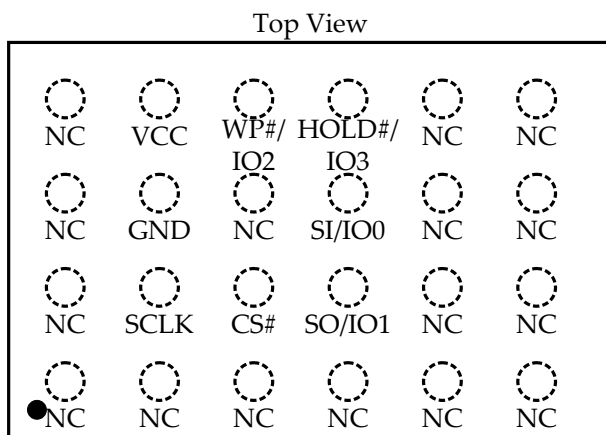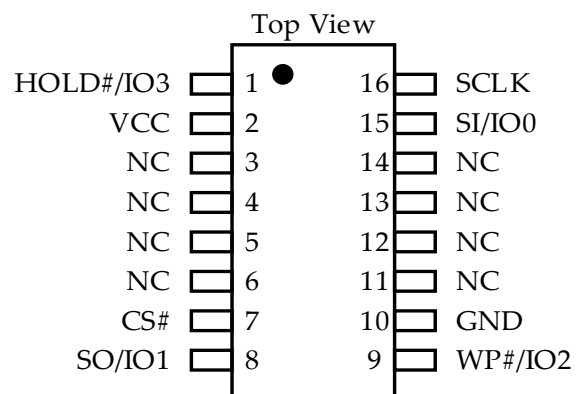
Figure 2: Pin Map

4. Pin Description

The NM25Q16A SPI Flash memory device operates with a single power supply of 3.3V typical.

Table 1: Pin Definitions

Signal	Direction	Description
CS#	Input	Chip Select, active low
SCLK	Input	Clock Input
SI/IO0	Input/Output	Serial Data Input in standard SPI; IO0 in Dual and Quad SPI
SO/IO1	Input/Output	Serial Data Output in standard SPI; IO1 in Dual and Quad SPI
WP#/IO2	Input/Output	Active low Write Protect in standard SPI; IO2 in Quad SPI
HOLD#/IO3	Input/Output	Active low Hold Input in standard SPI; IO3 in Quad SPI
VCC	-	Power Supply
GND	-	GND

4.1. Chip Select (CS#)

The Chip Select (CS#) pin enables and disables device operations.

When CS# is high, the device is deselected and all data output pins are at high impedance state; the device is in standby mode with standby level of power consumption if Write Status Register, program or erase operations are absent.

When CS# is low, the device is selected, available for incoming commands.

4.2. Clock Input (SCLK)

The clock input provides a reference of the synchronization of the SPI interface. All inputs are latched on the rising edge of SCLK, while all data shifts out on its falling edge.

4.3. Serial Input (SI/IO0)

Serial input is a unidirectional pin in Standard SPI mode, which is the input for all commands, data and address. In Dual and Quad SPI modes, SI functions as bidirectional IO0, which receives command, address and data as an input, and shifts out data as an output.

4.4. Serial Output (SO/IO1)

SO is unidirectional in Standard SPI mode for the output of all internal status and data. In Dual and Quad SPI modes, SO functions as bidirectional IO1, which receives data and address, and shifts out data.

4.5. Write Protect (WP#/IO2)

The WP# Write Protect function is available only if QE is 0. The WP# pin in conjunction with SRP0 bit protect the Status Register from unwanted modifications.

When QE is 1, Quad SPI mode is enabled, and if Quad SPI command is issued, then the WP# function is disabled and this pin functions as a dedicated IO2 data pin, which receives address and data, and also shifts out data.

4.6. HOLD (HOLD#/IO3)

The HOLD# function is available only if QE is 0. Driving the HOLD# pin low halts all serial communications

of the device, without affecting any ongoing WRSR, program or erase operations in progress. During hold state, all outputs are released to high impedance, and SI and SCLK are ignored by the device. Deasserting CS# while HOLD# is low will reset the internal logic of the device.

SCLK and HOLD# controls the entrance and exit of hold state. A falling edge of HOLD# during SCLK=0, or falling edge of SCLK during HOLD#=0 brings the device into HOLD state; a rising edge of HOLD# while SCLK=0, or falling edge of SCLK while HOLD#=1 brings the device out of HOLD state. The CS# should keep low during HOLD state.
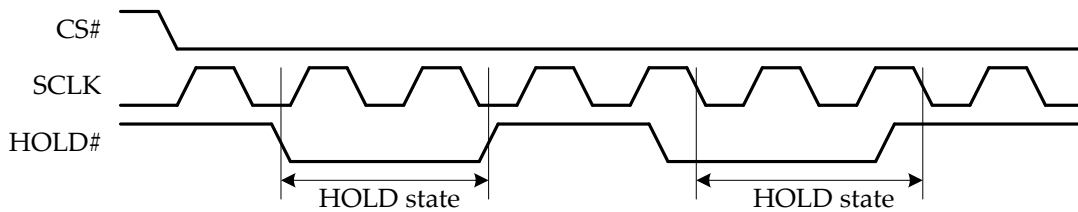
Figure 3: HOLD Condition

When QE is 1, Quad SPI is enabled, and if Quad SPI command is issued, then the HOLD# function is disabled and this pin functions as dedicated IO3 data pin, which receives data and address, and shifts out data.

While the device is in Quad SPI mode, tying the HOLD# pin directly to Vcc or GND is strictly forbidden to avoid signal conflict which may lead to permanent damage in the device.

5. Memory Organization and Operations

The NM25Q16A utilizes a variety of registers and memory array to store control information and user data, including: Identification, Status Register, Security Register, SFDP register, main memory array.

5.1. Identification

Table 2: Identification Definitions

Command	Comments	Manufacture ID (MID7 ~ MID0)	Memory Type (ID15 ~ ID8)	Memory Density (ID7 ~ ID0)	Device ID (ID7 ~ ID0)
----	----	94h	40h	16h	15h
9Fh	Read Identification	✓	✓	✓	----
90h/92h/94h	Read Manufacturer / Device ID	✓	----	----	✓
ABh	Read Device ID	----	----	----	✓

5.2. Status Register

Table 3: Status Register 3 (SR3)

Bit	S23	S22	S21	S20	S19	S18	S17	S16
Name	Reserved	DRV1	DRV0	HPF	Reserved	Reserved	Reserved	Reserved
R/W	----	R/W	R/W	R	----	----	----	----

Abbreviations used in Table 3 through Table 5:

(1) R/W: the bit can be read or written;

(2) R: the bit is read only

The SR3 register is read by 15h and written by 11h commands.

Table 4: Status Register 2 (SR2)

Bit	S15	S14	S13	S12	S11	S10	S9	S8
Name	SUS1	CMP	LB3	LB2	LB1	SUS2	QE	Reserved

R/W	R	R/W	R/W	R/W	R/W	R	R/W	----

The SR2 register is read by 35h and written by 31h commands.

Table 5: Status Register 1 (SR1)

Bit	S7	S6	S5	S4	S3	S2	S1	S0
Name	SRP0	BP4	BP3	BP2	BP1	BP0	WEL	WIP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

The SR1 register is read by 05h and written by 01h commands.

5.2.1.WIP Bit

Write In Progress Bit(WIP) indicates whether a WRSR, program or erase operation is in progress.

    0 = device is idle

    1 = device is busy in WRSR, program or erase operation

5.2.2.WEL Bit

Write Enable Latch Bit(WEL) indicates whether the device is ready to accept a WRSR, program or erase command.

    0 = WRSR, program or erase command is not accepted

    1 = WRSR, program or erase command is allowed

WEL is reset by:

(1) Power up;

(3) Write Disable (WRDI, 04h) command;

(2) Completion of WRSR, program or erase operations;

(4) Software Reset (66h+99h) command.

5.2.3.BP4, BP3, BP2, BP1, BP0 Bits

BP4 through BP0 are Block Protect bits. BP bits in combination with CMP bit define the protect scheme of the main memory array.

For details, see Table 13 and Table 14.

5.2.4.SRP0 Bit

Status Register Protect Bit(SRP0) and WP# pin control the protection scheme of Status Register.

For details, see Table 12.

5.2.5.QE Bit

QE Bit indicates whether the quad mode is enabled. When QE is 0, WP# and HOLD# pins are enabled. When QE is 1, Quad SPI operations enabled and WP#, HOLD# functions as IO2, IO3.

If WP# or HOLD# is tied directly to power supply or GND, then the QE bit should never be set to 1 to avoid signal conflict.

5.2.6.SUS2, SUS1 Bits

SUS2: Program Suspend Bit indicates whether a Program operation is in suspension. The bit is set to 1 by 75h command, cleared to 0 by 7Ah or 66h+99h commands, or powering up the device.

    0 = The device is not in Program suspension.

    1 = Program suspension in progress.

SUS1: The Erase Suspend Bit indicates whether an Erase operation is in suspension. The bit is set to 1 by 75h command, cleared to 0 by 7Ah or 66h+99h commands, or powering up the device.

    0 = The device is not in Erase suspension.

    1 = Erase suspension in progress.

5.2.7.LB3, LB2, LB1 Bits

LB3, LB2 and LB1 are the Lock Bits for Security Registers 3, 2 and 1, respectively.

    0 = The corresponding Security Register can be programmed/erased.

    1 = The corresponding Security Register is protected permanently.

LB3 through LB1 are OTP bits. Upon device delivery, they are default to 0. Programming from 0 to 1 is permanent.

LB3, LB2 and LB1 are can only be written by 06h command, but not can be written by 05h command.

5.2.8.CMP Bit

Complement Protect Bit(CMP), which in conjunction with Block Protect bits (BP4 through BP0) determines the protection scheme of the main memory array.

For details, see Table 13 and Table 14.

5.2.9.HPF Bit

High Performance Flag Bit indicates whether the device is in high performance mode.

    0 = Device is in normal mode.

    1 = Device is in high performance mode.

5.2.10.   DRV1, DRV0 Bits

DRV1 and DRV0 Bits control the drive strength which to determine the drive strength of output buffers in read operations.

    DRV1, DRV0 = 00: 100%

    DRV1, DRV0 = 01: 75% (default)

    DRV1, DRV0 = 10: 50%

    DRV1, DRV0 = 11: 25%

5.3. Security Register

Security Registers are three 1024-byte registers that can be individually protected by OTP programmable LB bits. Once a LB bit is set to 1, the corresponding Security Register becomes permanently locked and all program or erase operations are ignored.

These registers can be individually erased, programmed or read using 44h, 42h or 48h commands; they may be used as storage for security or other important information separately from the main memory array.

Table 6: Security Register Address Distribution

Security Register	A23-A16	A15-A12	A11-A10	A9-A0
Security Register #1	00h	000x	00	Byte Address
Security Register #2	00h	0010	00	Byte Address
Security Register #3	00h	0011	00	Byte Address

5.4. SFDP Register

The NM25Q16A features a 256-byte Serial Flash Discoverable Parameter (SFDP) register. It provides a

means to interrogate flash device characteristics and make appropriate adjustments while accessing the device.

The concept of SFDP Register definitions is similar to the JEDEC JESD216 standard (April 2011).

5.4.1. SFDP Header Information

Table 7: Signature and Parameter Identification Data Values

Description	Comment	Addr[1]	Bits[2]	Data[3]	Data[4]
SFDP Signature	Fixed:50444653h	00h	[07:00]	53h	53h
		01h	[15:08]	46h	46h
		02h	[23:16]	44h	44h
		03h	[31:24]	50h	50h
SFDP Minor Revision Number	Start from 00h	04h	[07:00]	00h	00h
SFDP Major Revision Number	Start from 01h	05h	[15:08]	01h	01h
Number of Parameters Headers	Start from 00h	06h	[23:16]	01h	01h
Unused	Contains 0xFFh and can never be changed	07h	[31:24]	FFh	FFh
ID number (JEDEC)	00h: A JEDEC specified header	08h	[07:00]	00h	00h
Parameter Table Minor Revision Number	Start from 0x00h	09h	[15:08]	00h	00h
Parameter Table Major Revision Number	Start from 0x01h	0Ah	[23:16]	01h	01h
Parameter Table Length (in double word)	Number of DWORDS in the Parameter table	0Bh	[31:24]	09h	09h
Parameter Table Pointer (PTP)	First address of JEDEC Flash Parameter table	0Ch	[07:00]	30h	30h
		0Dh	[15:08]	00h	00h
		0Eh	[23:16]	00h	00h
Unused	Contains 0xFFh and can never be changed.	0Fh	[31:24]	FFh	FFh
ID Number (NeuMem Manufacturer ID)	Indicates NeuMem manufacturer ID	10h	[07:00]	94h	94h
Parameter Table Minor Revision Number	Start from 0x00h	11h	[15:08]	00h	00h
Parameter Table Major Revision Number	Start from 0x01h	12h	[23:16]	01h	01h
Parameter Table Length (in double word)	Number of DWORDS in the Parameter table	13h	[31:24]	03h	03h
Parameter Table Pointer (PTP)	First address of NeuMem Flash Parameter table	14h	[07:00]	60h	60h
		15h	[15:08]	00h	00h
		16h	[23:16]	00h	00h
Unused	Contains 0xFFh and can never be changed	17h	[31:24]	FFh	FFh

Notes:

1. The "Addr" column indicates the byte address in SFDP area.
2. The "Bits" column is the bit range of the specified data within a 32-bit-word which comprises four consecutive 8-bit bytes.
3. This column is the data expressed in binary (with suffix "b") or hexadecimal (with suffix "h").
4. This column is the data in hexadecimal, as is indicated by the suffix "h".

5.4.2.Parameter Table (0)

Table 8: Parameter Table (0): JEDEC Flash Parameter Tables

Description	Comment	Addr	Bits	Data	Data
Block/Sector Erase Size	00: Reserved; 01: 4KB Erase; 10: Reserved; 11: do not support 4KB erase	30h	[01:00]	01b	E5h
Write Granularity	0: 1Byte, 1: 64Byte or larger		[02]	1b	
Write Enable Instruction Required for Writing to Volatile Status Register	0: Nonvolatile status bit 1: Volatile status bit		[03]	0b	
Write Enable Opcode Select for Writing to Volatile Status Registers	0: Use 50h Opcode; 1: Use 06h Opcode. Note: If target flash status register is Nonvolatile, then bits 3 and 4 must be set to 00b.		[04]	0b	
Unused	Contains 111b and can never be changed		[07:05]	111b	
4KB Erase Opcode		31h	[15:08]	20h	20h
(1-1-2) Fast Read	0=Not supported 1=Supported	32h	[16]	1b	F1h
Number of Address Bytes used in addressing flash array	00: 3-Byte only; 01: 3- or 4-Byte; 10: 4-Byte only; 11: Reserved		[18:17]	00b	
Double Transfer Rate (DTR) clocking	0=Not supported 1=Supported		[19]	0b	
(1-2-2) Fast Read	0=Not supported 1=Supported		[20]	1b	
(1-4-4) Fast Read	0=Not supported 1=Supported		[21]	1b	
(1-1-4) Fast Read	0=Not supported 1=Supported		[22]	1b	
Unused	----		[23]	1b	
Unused	----	33h	[31:24]	FFh	FFh
Flash Memory Density		37h: 34h	[31:00]	001F_FFFFh	
(1-4-4) Fast Read Number of Wait states	0_0000b: Wait states (dummy clocks) not supported	38h	[04:00]	0_0100b	44h
(1-4-4) Fast Read Number of Mode Bits	000b: Mode Bits not supported		[07:05]	010b	
(1-4-4) Fast Read Opcode		39h	[15:08]	EBh	EBh
(1-1-4) Fast Read Number of Wait states	0_0000b: Wait states (Dummy Clocks) not supported	3Ah	[20:16]	0_1000b	08h
(1-1-4) Fast Read Number of Mode Bits	000b: Mode Bits not supported		[23:21]	000b	

(1-1-4) Fast Read Opcode		3Bh	[31:24]	6Bh	6Bh
(1-1-2) Fast Read Number of Wait states	0_0000b: Wait states (Dummy Clocks) not supported	3Ch	[04:00]	0_1000b	08h
(1-1-2) Fast Read Number of Mode Bits	000b: Mode Bits not supported		[07:05]	000b	
(1-1-2) Fast Read Opcode		3Dh	[15:08]	3Bh	3Bh
(1-2-2) Fast Read Number of Wait states	0_0000b: Wait states (Dummy Clocks) not supported	3Eh	[20:16]	0_0000b	40h
(1-2-2) Fast Read Number of Mode Bits	000b: Mode Bits not supported		[23:21]	010b	
(1-2-2) Fast Read Opcode		3Fh	[31:24]	BBh	BBh
(2-2-2) Fast Read	0: Not supported 1: Supported	40h	[00]	0b	EEh
Unused	----		[03:01]	111b	
(4-4-4) Fast Read	0: Not supported 1: Supported		[04]	0b	
Unused	----		[07:05]	111b	
Unused	----	43h: 41h	[31:08]	0xFFh	0xFFh
Unused	----	45h: 44h	[15:00]	0xFFh	0xFFh
(2-2-2) Fast Read Number of Wait states	0_0000b: Wait states (Dummy Clocks) not supported	46h	[20:16]	00000b	00h
(2-2-2) Fast Read Number of Mode Bits	000b: Mode Bits not supported		[23:21]	000b	
(2-2-2) Fast Read Opcode		47h	[31:24]	FFh	FFh
Unused	----	49h: 48h	[15:00]	0xFFh	0xFFh
(4-4-4) Fast Read Number of Wait states	0_0000b: Wait states (Dummy Clocks) not supported	4Ah	[20:16]	0_0000b	00h
(4-4-4) Fast Read Number of Mode Bits	000b: Mode Bits not supported		[23:21]	000b	
(4-4-4) Fast Read Opcode		4Bh	[31:24]	FFh	FFh
Sector Type 1 Size	0x00b: Sector type doesn't exist N: sector/block size = 2^N bytes	4Ch	[07:00]	0Ch	0Ch
Sector Type 1 erase Opcode		4Dh	[15:08]	20h	20h
Sector Type 2 Size	0x00b: Sector type doesn't exist N: sector/block size = 2^N bytes	4Eh	[23:16]	0Fh	0Fh
Sector Type 2 erase Opcode		4Fh	[31:24]	52h	52h
Sector Type 3 Size	0x00b: Sector type doesn't exist N: sector/block size = 2^N bytes	50h	[07:00]	10h	10h
Sector Type 3 erase Opcode		51h	[15:08]	D8h	D8h
Sector Type 4 Size	0x00b: Sector type doesn't exist N: sector/block size = 2^N bytes	52h	[23:16]	00h	00h
Sector Type 4 erase Opcode		53h	[31:24]	FFh	FFh

5.4.3.Parameter Table (1)

Table 9: Parameter Table (1): NeuMem Flash Parameter Tables

Description	Comment	Addr	Bits	Data	Data
Vcc Supply Maximum Voltage	2000h=2.000V 2700h=2.700V 3600h=3.600V	61h: 60h	[15:00]	3600h	3600h
Vcc Supply Minimum Voltage	1650h=1.650V 2250h=2.250V 2350h=2.350V 2700h=2.700V	63h: 62h	[31:16]	2700h	2700h
Hardware Reset# pin	0 = Not supported 1 = Supported	65h: 64h	[00]	0b	F99Eh
Hardware Hold# pin	0 = Not supported 1 = Supported		[01]	1b	
Deep Power Down Mode	0 = Not supported 1 = Supported		[02]	1b	
Software Reset	0 = Not supported 1 = Supported		[03]	1b	
Software Reset Opcode	(Reset Enable 66h should be issued before Reset Opcode)		[11:04]	99h	
Program Suspend/Resume	0 = Not supported 1 = Supported		[12]	1b	
Erase Suspend/Resume	0 = Not supported 1 = Supported		[13]	1b	
Unused	----		[14]	1b	
Wrap-Around Read mode	0 = Not supported 1 = Supported		[15]	1b	
Wrap-Around Read mode Opcode		66h	[23:16]	77h	77h
Wrap-Around Read data length	08h: Support 8B wrap-around read 16h: 8B & 16B 32h: 8B & 16B & 32B 64h: 8B & 16B & 32B & 64B	67h	[31:24]	64h	64h
Individual block lock	0 = Not supported 1 = Supported	6Bh: 68h	[00]	0b	EBFCh
Individual block lock bit (Volatile/Nonvolatile)	0 = Volatile 1 = Nonvolatile		[01]	0b	
Individual block lock Opcode			[09:02]	FFh	
Individual block lock Volatile protect bit default protect status	0 = Protect 1 = Unprotect		[10]	0b	
Secured OTP	0 = Not supported 1 = Supported	6Bh: 68h	[11]	1b	EBFCh
Read Lock	0 = Not supported 1 = Supported		[12]	0b	

Permanent Lock	0 = Not supported 1 = Supported		[13]	1b	
Unused	----		[15:14]	11b	
Unused	----		[31:16]	FFFFh	FFFFh

5.5. Main Array

5.5.1.Address Space Distribution of Main Array

Table 10: NM25Q16A Memory Organization

A device has	A 64KB Block has	A 32KB Block has	A sector has	A page has	--
32	1	--	--	--	64KB Blocks
64	2	1	--	--	32KB Blocks
512	16	8	1	--	4KB Sectors
8192	256	128	16	1	Pages
2097152 (2M)	65536	32768	4096	256	Bytes

All blocks or sectors of the memory are of uniform size; the address distribution of NM25Q16A is offered below.

Table 11: NM25Q16A Address Distribution

Chip Capacity	64KB Block	32KB Block	Sector	Address Range
16M bit or 2M byte	31	63	511	1F_F000h ~ 1F_FFFFh
			……	……
			504	1F_8000h ~ 1F_8FFFh
		62	503	1F_7000h ~ 1F_7FFFh
			……	……
			496	1F_0000h ~ 1F_0FFFh
	30	61	495	1E_F000h ~ 1E_FFFFh
			……	……
			488	1E_8000h ~ 1E_8FFFh
		60	487	1E_7000h ~ 1E_7FFFh
			……	……
			480	1E_0000h ~ 1E_0FFFh
	……	……	……	……
	……	……	……	……
	1	3	31	01_F000h ~ 01_FFFFh
			……	……
			24	01_8000h ~ 01_8FFFh
		2	23	01_7000h ~ 01_7FFFh
			……	……
			16	01_0000h ~ 01_0FFFh
	0	1	15	00_F000h ~ 00_FFFFh
			……	……
			8	00_8000h ~ 00_8FFFh
		0	7	00_7000h ~ 00_7FFFh
			……	……
			0	00_0000h ~ 00_0FFFh

6. SPI Operation

6.1. Standard SPI

Standard SPI has a four signal bus: CS#, SCLK, SI and SO. Both mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

6.2. Dual SPI

The device supports Dual SPI operations for the following commands:

"Dual Output Fast Read" (3Bh);

"Dual I/O Fast Read" (BBh);

"Read Manufacture ID / Device ID Dual I/O" (92h).

During these commands, SI and SO pins become IO0 and IO1. Data is transferred using IO0 and IO1, doubling the throughput of Standard SPI mode.

6.3. Quad SPI

The device supports Quad SPI operation for the following commands:

"Quad Output Fast Read" (6Bh);

"Quad I/O Fast Read" (EBh);

"Quad I/O Word Fast Read" (E7h);

"Read Manufacture ID / Device ID Quad I/O" (94h);

"Quad Page Program" (32h).

During these commands, SI, SO, WP# and HOLD# become IO0, IO1, IO2 and IO3, respectively. Data is transferred using IO0 through IO3, offering four times the throughput of Standard SPI mode.

As a prerequisite, the QE bit in Status Register must be set to 1 prior to Quad SPI commands. If Quad SPI is activated, it is strictly forbidden to tie WP# and HOLD# to power supply or GND to prevent signal conflict which may damage the device permanently.

7. Data Protection

As a nonvolatile memory device the NM25Q16A may suffer from the compromise of data integrity in the event of noise and other adverse system conditions. To improve the robustness of the device, certain methods are adopted to protect the data from inadvertent WRSR, program or erase operations.

7.1. Write Protect Features

NM25Q16A offers the following protection schemes.

(1) The device is reset when Vcc is below threshold.

(2) Write is disabled for a duration after device is power-up.

(3) Prior to WRSR, program or erase operations, a Write Enable (WREN) command is needed to set WEL bit to 1; after these operations are complete, the WEL bit returns to 0.

This mechanism ensures that the memory content can be changed only after specific command sequence is successfully completed.

(4) Software Protection Mode: The CMP, BP4, BP3, BP2, BP1 and BP0 bits define the address space in the main memory array that is under protection. The protected area can only be read out; program or erase operations to protected area are ignored.

For details, see Table 13 and Table 14.

(5) Hardware Protection Mode: WP# pin and SRP0 bit protect Status Register bits from modifications.

For details, see Table 12.

(6) While in Deep Power-Down Mode, the device ignores all commands except Release from Deep

Power-Down Mode (ABh). This protects the device from all WRSR, program or erase commands.

7.2. Status Register Protection

SRP0 bit in the Status Register and WP# pin provide protection for the Status Register itself.

Table 12: Status Register Protection Scheme

SRP0	WP#	Protection Scheme	Description
0	x	Software Protected	Status Register is unlocked and can be written to after a Write Enable command which Sets WEL=1.(Default)
1	0	Hardware Protected	Status Register is locked and cannot be written to.
1	1	Hardware Unprotected	Status Register is unlocked and can be written to after a Write Enable command which Sets WEL=1.

7.3. Main Memory Array Protection

A combination of Status Register bits define the area space of the memory array that is protected from program and erase operations. A program operation targeted at a page address that is under protection is not executed. For erase operations, if any address location within the designated target area is protected then the command is not executed.

7.3.1. CMP=0

Table 13: NM25Q16A Memory Protection pattern (CMP=0)

Status Register Bits						Memory Space in Protection			
CMP	BP4	BP3	BP2	BP1	BP0	Blocks	Address Range	Density	Portion
0	x	x	0	0	0	None	None	None	None
0	0	0	0	0	1	None	None	None	None
0	0	0	0	1	0	None	None	None	None
0	0	0	0	1	1	None	None	None	None
0	0	0	1	0	0	None	None	None	None
0	0	0	1	0	1	None	None	None	None
0	0	0	1	1	0	None	None	None	None
0	0	1	0	0	1	0	00_0000h ~ 00_FFFFh	64KB	Lower 1/64
0	0	1	0	1	0	0 to 1	00_0000h ~ 01_FFFFh	128KB	Lower 1/32
0	0	1	0	1	1	0 to 3	00_0000h ~ 03_FFFFh	256KB	Lower 1/16
0	0	1	1	0	0	0 to 7	00_0000h ~ 07_FFFFh	512KB	Lower 1/8
0	0	1	1	0	1	0 to 15	00_0000h ~ 0F_FFFFh	1MB	Lower 1/4
0	0	1	1	1	0	0 to 31	00_0000h ~ 1F_FFFFh	2MB	All
0	x	x	1	1	1	0 to 31	00_0000h ~ 1F_FFFFh	2MB	All
0	1	0	0	0	1	None	None	None	None
0	1	0	0	1	0	None	None	None	None
0	1	0	0	1	1	None	None	None	None
0	1	0	1	0	x	None	None	None	None
0	1	0	1	1	0	None	None	None	None
0	1	1	0	0	1	0	00_0000h ~ 00_0FFFh	4KB	Bottom Block
0	1	1	0	1	0	0	00_0000h ~ 00_1FFFh	8KB	Bottom Block

0	1	1	0	1	1	0	00_0000h ~ 00_3FFFh	16KB	Bottom Block
0	1	1	1	0	x	0	00_0000h ~ 00_7FFFh	32KB	Bottom Block
0	1	1	1	1	0	0	00_0000h ~ 00_7FFFh	32KB	Bottom Block

7.3.2. CMP=1

The CMP bit offers more flexibility in memory protection, as is shown below.

Table 14: NM25Q16A Memory Protection pattern (CMP=1)

Status Register Bits						Memory Space in Protection			
CMP	BP4	BP3	BP2	BP1	BP0	Blocks	Address Range	Density	Portion
1	x	x	0	0	0	All	00_0000h ~ 1F_FFFFh	2MB	All
1	0	0	0	0	1	0 to 31	00_0000h ~ 1F_FFFFh	2MB	All
1	0	0	0	1	0	0 to 31	00_0000h ~ 1F_FFFFh	2MB	All
1	0	0	0	1	1	0 to 31	00_0000h ~ 1F_FFFFh	2MB	All
1	0	0	1	0	0	0 to 31	00_0000h ~ 1F_FFFFh	2MB	All
1	0	0	1	0	1	0 to 31	00_0000h ~ 1F_FFFFh	2MB	All
1	0	0	1	1	0	0 to 31	00_0000h ~ 1F_FFFFh	2MB	All
1	0	1	0	0	1	1 to 31	01_0000h ~ 1F_FFFFh	1984KB	Upper 31/32
1	0	1	0	1	0	2 to 31	02_0000h ~ 1F_FFFFh	1920KB	Upper 15/16
1	0	1	0	1	1	4 to 31	04_0000h ~ 1F_FFFFh	1792KB	Upper 7/8
1	0	1	1	0	0	8 to 31	08_0000h ~ 1F_FFFFh	1536KB	Upper 3/4
1	0	1	1	0	1	16 to 31	10_0000h ~ 1F_FFFFh	1MB	Upper 1/2
1	0	1	1	1	0	None	None	None	None
1	x	x	1	1	1	None	None	None	None
1	1	0	0	0	1	0 to 31	00_0000h ~ 1F_FFFFh	All	All
1	1	0	0	1	0	0 to 31	00_0000h ~ 1F_FFFFh	All	All
1	1	0	0	1	1	0 to 31	00_0000h ~ 1F_FFFFh	All	All
1	1	0	1	0	x	0 to 31	00_0000h ~ 1F_FFFFh	All	All
1	1	0	1	1	0	0 to 31	00_0000h ~ 1F_FFFFh	All	All
1	1	1	0	0	1	0 to 31	00_1000h ~ 1F_FFFFh	2044KB	U[2] 511/512
1	1	1	0	1	0	0 to 31	00_2000h ~ 1F_FFFFh	2040KB	U 255/256
1	1	1	0	1	1	0 to 31	00_4000h ~ 1F_FFFFh	2032KB	U 127/128
1	1	1	1	0	x	0 to 31	00_8000h ~ 1F_FFFFh	2016KB	U 63/64
1	1	1	1	1	0	0 to 31	00_8000h ~ 1F_FFFFh	2016KB	U 63/64

Notes:

1. "L" is short for "Lower".
2. "U" is short for "Upper".

8. Command Definitions

All commands, addresses and data are shifted in and out of the device, beginning with the MSB of the command opcode. All inputs are latched into the device on SCLK rising edge, while all outputs are shifted out on SCLK falling edge.

Every command sequence starts with a one-byte command code. Depending on the command, the command code might be followed by address bytes, data bytes, dummy bytes, or a combination. CS# must

be driven high after the last bit of the command sequence is completed.

Read-related commands (Read, Fast Read, Read Status Register or Release from Deep Power-Down, Read Device ID) shifts out data from the device. CS# can be driven high after any bit of the output data sequence. For other commands including Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable or Deep Power-Down, CS# must be driven high exactly at a byte boundary; otherwise if CS# is driven high at any time when the input byte is not a full byte, the command is ignored and WEL will not be reset.

Table 15: Command Definitions (Standard SPI, Dual SPI, Quad SPI)

Command	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
Enable Reset	66h						
Reset	99h						
Read Unique ID	4Bh	dummy	dummy	dummy	dummy	UID63-UID0	(continuous)
Read Manufacturer / Device ID	90h	dummy	dummy	00H	(MID7-MID0)	DID7-DID0	(continuous)
Read Manufacturer / Device ID by Dual I/O	92h	A23-A8	A7-A0, M7-M0	(MID7-MID0) (DID7-DID0)			(continuous)
Read Manufacturer / Device ID by Quad I/O	94h	A23-A0, M7-M0	dummy (10) (MID7-MID0) (DID7-DID0)				(continuous)
Read Identification	9Fh	MID7-MID0	JDID15-JDID8	JDID7-JDID0			(continuous)
Write Enable	06h						
Write Disable	04h						
Read Data	03h	A23-A16	A15-A8	A7-A0	D7-D0	(Next byte)	(continuous)
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	dummy	D7-D0	(continuous)
Dual Output Fast Read	3Bh	A23-A16	A15-A8	A7-A0	dummy	D7-D0	(continuous)
Dual I/O Fast Read	BBh	A23-A8	A7-A0, M7-M0	D7-D0	(Next byte)	(Next byte)	(continuous)
Quad Output Fast Read	6Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(continuous)
Quad I/O Fast Read	EBh	A23-A0, M7-M0	dummy	D7-D0	(Next byte)	(Next byte)	(continuous)
Quad I/O Word Fast Read	E7h	A23-A0, M7-M0	dummy	D7-D0	(Next byte)	(Next byte)	(continuous)
Volatile SR Write Enable	50h						
Read Status Register-1	05h	S7-S0					(continuous)
Read Status Register-2	35h	S15-S8					(continuous)
Read Status Register-3	15h	S23-S16					(continuous)
Write Status Register-1	01h	S7-S0					

Write Status Register-2	31h	S15-S8					
Write Status Register-3	11h	S23-S16					
Erase Security Registers	44h	A23-A16	A15-A8	A7-A0			
Program Security Registers	42h	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0	(continuous)
Read Security Registers	48h	A23-A16	A15-A8	A7-A0	dummy	D7-D0	(continuous)
Set Burst with Wrap	77h	dummy, W7-W0					
Program/Erase Suspend	75h						
Program/Erase Resume	7Ah						
Read Serial Flash Discoverable Parameter	5Ah	A23-A16	A15-A8	A7-A0	dummy	D7-D0	(continuous)
Sector Erase	20h	A23-A16	A15-A8	A7-A0			
Block Erase (32KB)	52h	A23-A16	A15-A8	A7-A0			
Block Erase (64KB)	D8h	A23-A16	A15-A8	A7-A0			
Chip Erase	C7h/ 60h						
Page Program	02h	A23-A16	A15-A8	A7-A0	D7-D0	(Next byte)	(continuous)
Quad Page Program	32h	A23-A16	A15-A8	A7-A0	D7-D0	(Next byte)	(continuous)
Fast Page Program	F2h	A23-A16	A15-A8	A7-A0	D7-D0	(Next byte)	(continuous)
High Performance Mode	A3h	dummy	dummy	dummy			
Release From Deep Power-Down or High Performance Mode, and Read Device ID	ABh	dummy	dummy	dummy	(DID7-DID0)		(continuous)
Release From Deep Power-Down	ABh						
Deep Power-Down	B9h						

Note: In read memory command, the next byte will be invalid data when read address in chip boundary.

8.1. Write Enable (WREN) (06h)

The WREN command sets the WEL bit to 1, which is a prerequisite prior to the following commands:

    Write Status Register (01h, 31h, 11h)

    Page Program (02h), Quad Page Program (32h), Fast Page Program (F2h)

    Sector Erase (20h), 32KB Block Erase (52h), 64KB Block Erase(D8h), Chip Erase (60h, C7h)

    Program Security Register (44h), Erase Security Register(42h)

These commands are ignored by the device without prior WREN command.

Command sequence:

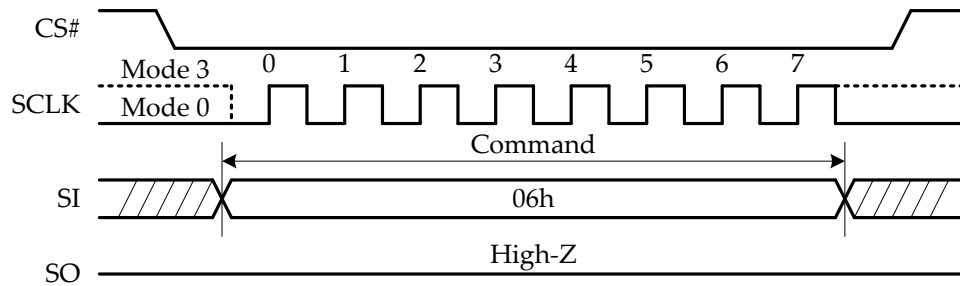CS# goes low --> Send 06h command into SI pin --> CS# goes high.

Figure 4: Write Enable (WREN) (06h) Command Sequence

8.2. Write Disable (WRDI) (04h)

The WRDI command resets the WEL bit to 0. The WEL bit is reset by the following operations:

   Power-up

   WRDI command (04h)

   Completion of Write Status Register

   Completion of Page Program (02h), Quad Page Program (32h), Fast Page Program (F2h)

   Completion of Sector Erase (20h), 32KB Block Erase (52h), 64KB Block Erase(D8h), Chip Erase (60h, C7h)

   Completion of Program Security Register (44h), Erase Security Register(42h)

   Reset command (66h+99h)

Command Sequence:

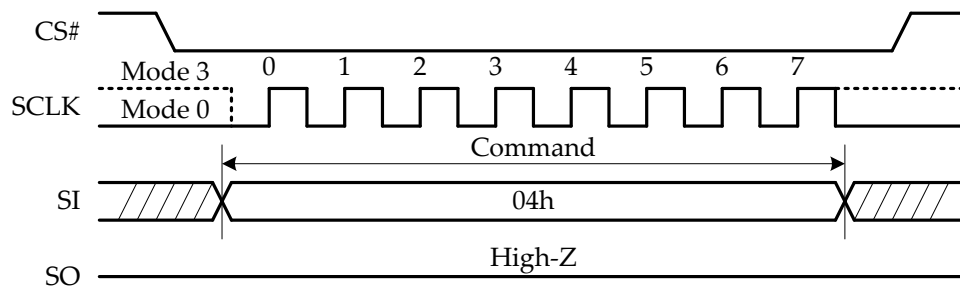Drive CS# low --> Send 04h command into SI pin --> Drive CS# high.

Figure 5: Write Disable (WRDI) (04h) Command Sequence

8.3. Write Enable for Volatile Status Register (50h)

The nonvolatile bits in the Status Register can also be written as volatile bits. This enables the host to quickly change the Status Register bits without the lengthy write cycle of nonvolatile bits, and it does not affect the endurance of the nonvolatile bits in the Status Register.

The 50h command does not set the WEL bit. It must be issued prior to WRSR command (01h, 31h or 11h); there should be no other commands inserted between 50h and WRSR command.

Command sequence:

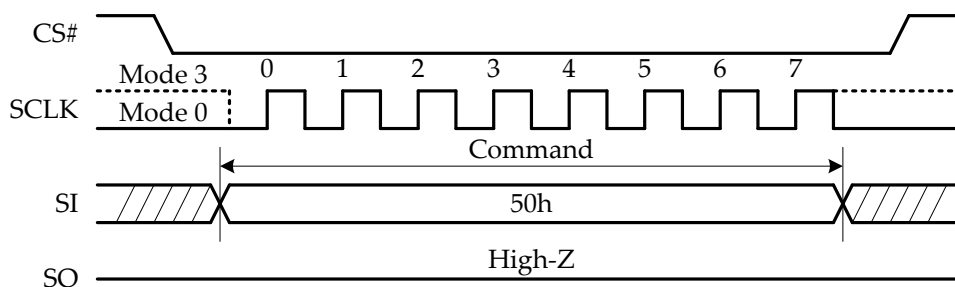Drive CS# low --> Send 50h command into SI pin --> Drive CS# high.

Figure 6: Write Enable for Volatile Status Register (50h) Command Sequence

8.4. Read Status Register (RDSR) (05h or 35h or 15h)

The RDSR commands enables the host to read out the Status Register. This command can be issued anytime, even while a WRSR, program or erase operation is in progress. It is recommended to use RDSR command to check the WIP bit before the next command is issued to the device.

The commands 05h, 35h and 15h reads SR1 (S7~S0), SR2 (S15~S8) and SR3 (S23~S16), respectively. While CS# remains low, an RDSR command can output the designated Status Register continuously.

Command sequence:

Drive CS# low --> Send RDSR command into SI pin --> Receive output data on SO pin --> Drive CS# high.
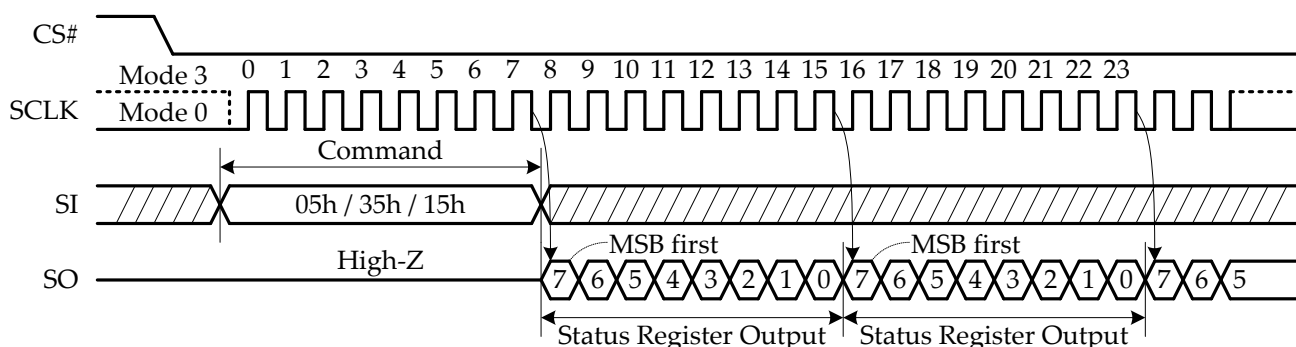

Figure 7: Read Status Register (RDSR) (05h or 35h or 15h) Command Sequence

8.5. Write Status Register (WRSR) (01h or 31h or 11h)

The WRSR command changes the values of Status Register. Before issuing WRSR command, a WREN command is needed to set the WEL bit.

The commands 01h, 31h and 11h writes SR1 (S7~S0), SR2 (S15~S8) and SR3 (S23~S16), respectively.

Within the Status Register, read-only and reserved bits are not affected by WRSR command. Also, following the rules specified in Table 12, a combinations of SRP0 bit and WP# pin may protect the Status Register against any write operations.

For the WRSR command to take effect, CS# must be deasserted exactly at a byte boundary, otherwise the command is ignored. After CS# is driven high, a duration of t_W is required before self-timed write cycle is complete. During t_W, the host may read the Status Register to check WIP bit. WIP is 1 if the device is busy in the write cycle; when the process completes and the device is ready to accept new commands, WIP and WEL are both reset to 0.

Command sequence:

Drive CS# low --> Send WRSR command into SI pin --> Send write data into SI pin --> Drive CS# high.
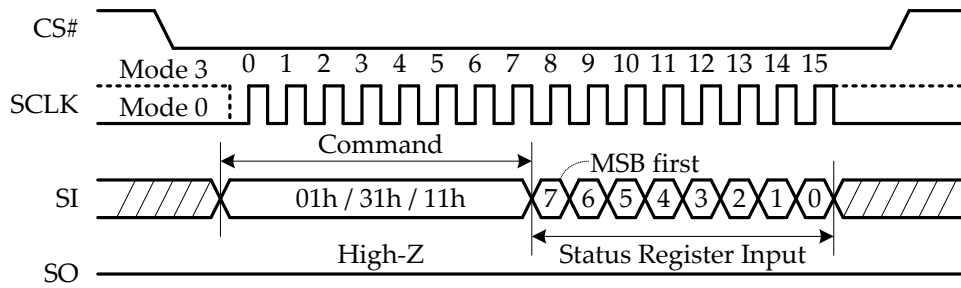
Figure 8: Write Status Register (WRSR) (01h or 31h or 11h) Command Sequence

8.6. Read Data Bytes (READ) (03h)

The READ command requires a 3-byte address (A23~A0) following the 03h command; the address can point to any location in the main memory array. Command and address are latched in on SCLK rising edge, and output data shifts out on SCLK falling edge. After each byte is shifted out, the address automatically increments to the next byte location; therefore, the entire memory can be output with a single READ command.

Maximum SCLK frequency of READ command is f_R. The command is rejected if a WRSR, program or erase operation is in progress.

Command sequence:

Drive CS# low --> Send 03h command into SI pin --> Send 24-bit address into SI pin --> Receive output data on SO pin --> Drive CS# high.
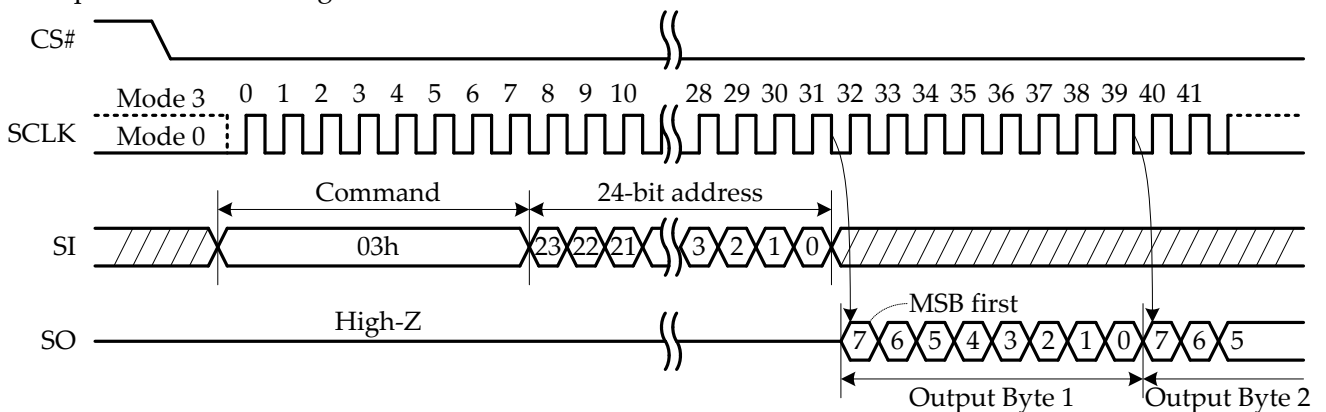

Figure 9: Read Data Bytes (READ) (03h) Command Sequence

8.7. Read Data Bytes at Higher Speed (Fast Read) (0Bh)

The Fast Read command has one more dummy byte after the 3-byte address compared with the READ command. Command and address are latched in on SCLK rising edge; output data shifts out on SCLK falling edge at a maximum clock frequency of f_{C3}.

Command sequence:

Drive CS# low --> Send 0Bh command into SI pin --> Send 24-bit address into SI pin --> 8 dummy SCLK cycles --> Receive output data on SO pin --> Drive CS# high.
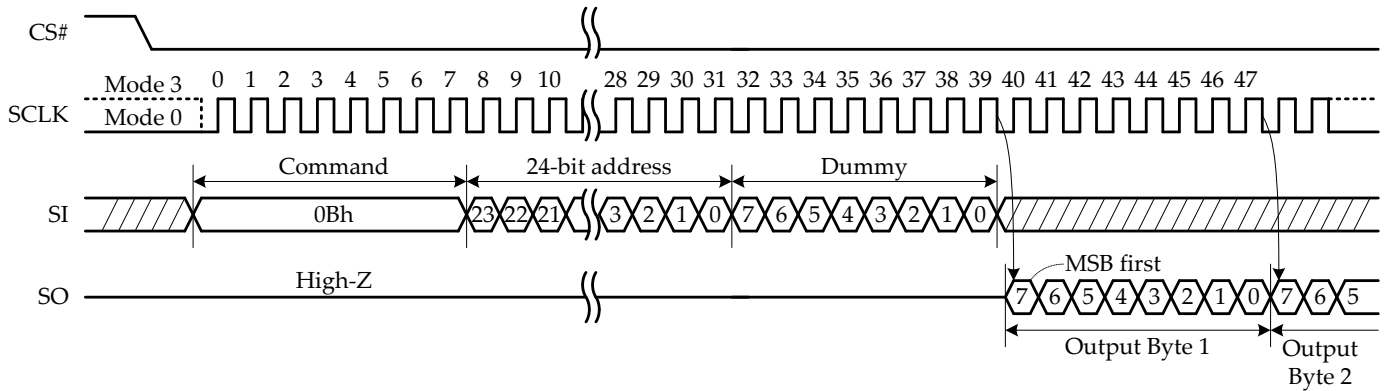
Figure 10: Read Data Bytes at Higher Speed (Fast Read) (0Bh) Command Sequence

8.8. Dual Output Fast Read (3Bh)

The 3Bh command is followed by 3-byte address and a dummy byte, and then two bits of data is shifted out per SCLK cycle on SI and SO pins. The address can point to any location in the main memory array, and it automatically increments to the next byte address after each byte of data is shifted out.

During the execution of 3Bh command, SI is a bidirectional IO which first acts as an input of command and address and then becomes an output for read data.

Figure 11: Dual Output Fast Read (3Bh) Command Sequence

8.9. Quad Output Fast Read (6Bh)

The 6Bh command is followed by 3-byte address and 8 dummy clocks, and outputs fours bits of data through IO3, IO2, IO1 and IO0 on each falling edge of SCLK. The first address can be any location in the main memory array; it automatically increments to the next byte address after each byte of data is shifted out.

The QE bit should be set before the 6Bh command is issued.

During the execution of 6Bh command, SI is a bidirectional IO which first acts as an input of command and address and then becomes an output for read data.
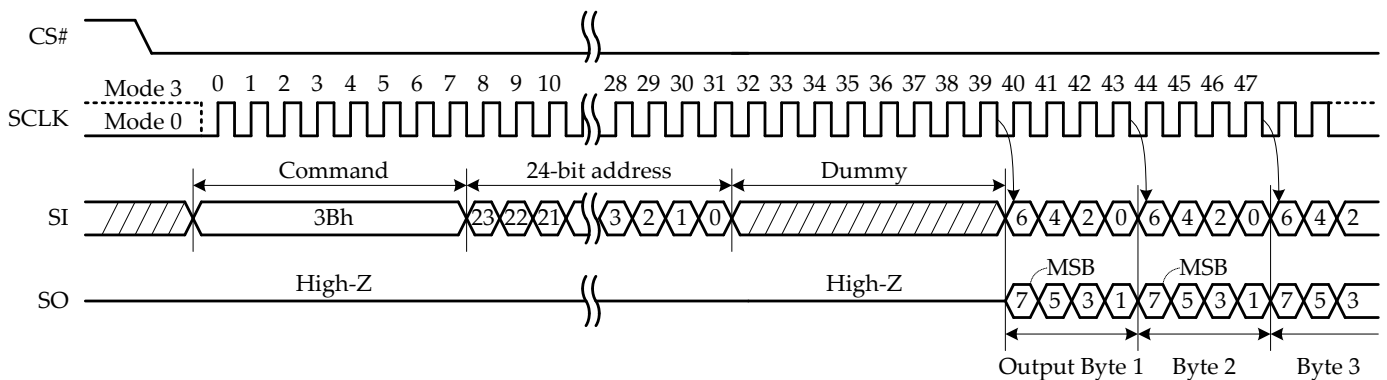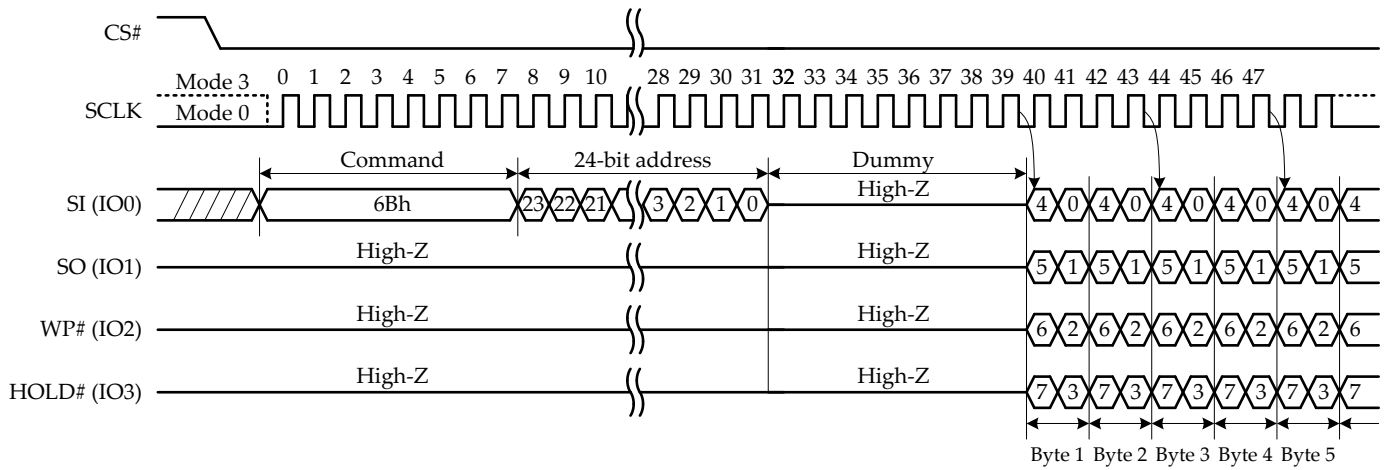
Figure 12: Quad Output Fast Read (6Bh) Command Sequence

8.10. Dual I/O Fast Read (BBh)

The BBh command is followed by 3-byte address and a "Continuous Read Mode" byte. Two dummy clocks are inserted. Address bytes and Mode bytes are latched in 2 bits per SCLK cycle on SI and SO pins, and then the memory content is shifted out 2 bits per clock cycle on the falling edge of SCLK. The first byte addressed can be at any location. The address automatically increments to the next byte after each byte is shifted out. The "Continuous Read Mode" bits can further reduce command overhead. If (M5, M4) are (1, 0), then the command word BBh is not required for the next Dual I/O Fast Read command; otherwise, the device returns to normal operation mode and requires explicit command word for the next instruction. A Software Reset command (66h+99h) can reset (M5, M4) and bring the device back to normal operation.
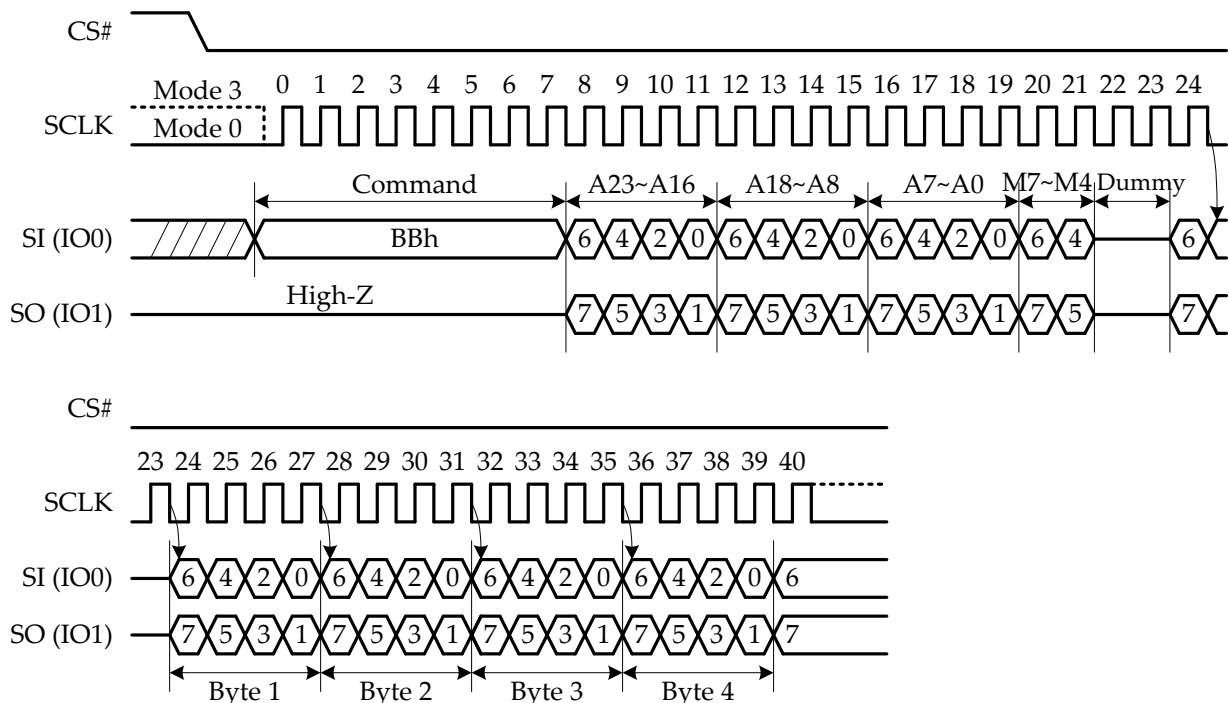

Figure 13: Dual I/O Fast Read (BBh) Command Sequence, (M5, M4) ≠ (1, 0)

8.10.1. Continuous Read Mode

If a previous BBh command has already set (M5, M4) to (1, 0), then the next Dual I/O Fast Read operation does not need the BBh opcode.
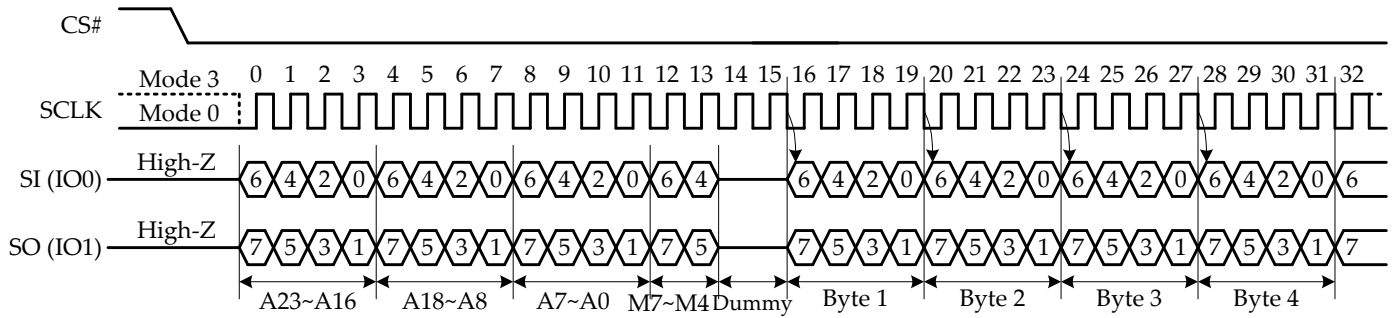
Figure 14: Dual I/O Fast Read (BBh) Command Sequence, (M5, M4) = (1, 0)

8.11. Quad I/O Fast Read (EBh)

The EBh command is similar to the BBh command except that it uses all four data pins IO0, IO1, IO2 and IO3 for address input, Continuous Read Mode bits input, dummy cycles and all output data bytes.
The QE bit must be set to 1 prior to EBh command.
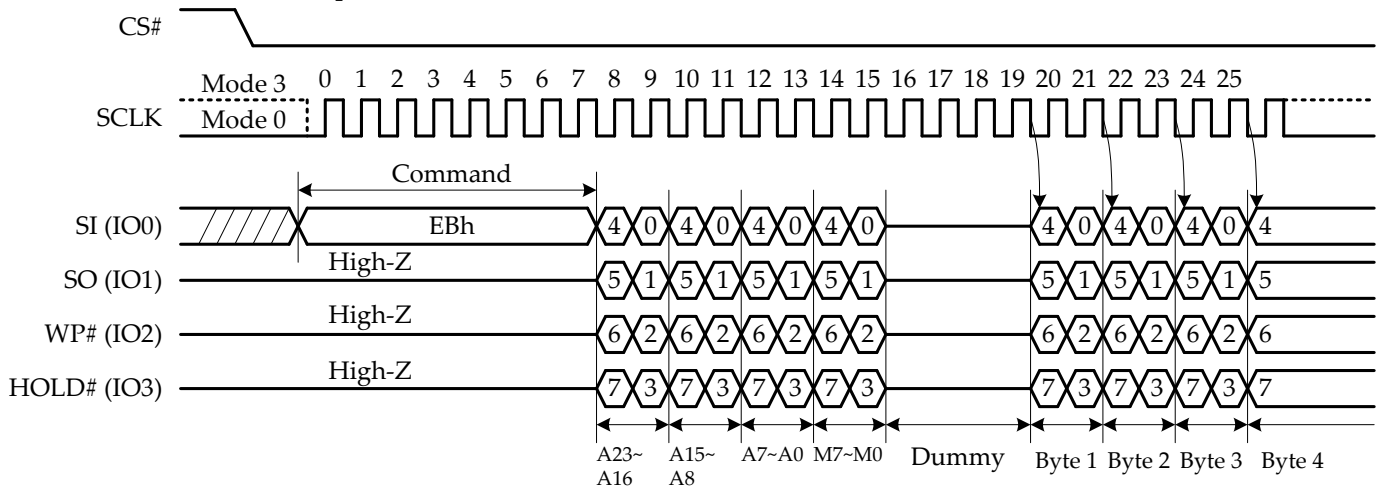
Figure 15: Quad I/O Fast Read (EBh) Command Sequence, (M5, M4) ≠ (1, 0)

8.11.1.   Continuous Read Mode

The Quad I/O Fast Read command can further reduce command overhead by setting the "Continuous Read Mode" bits (M7-M0) after the 3-byte address (A23-A0).

If (M5~M4) of the current transfer is (1, 0), then the next operation after CS# toggles high and then low is automatically recognized as Quad I/O Fast Read and does not require an explicit EBh opcode; otherwise, if (M5~M4) of the current transfer is not (1, 0), then the device keeps in normal state and requires an explicit input of command word for the next operation.

The Software Reset (66h+99h) command resets (M5~M4) bits and brings the device back to normal state.
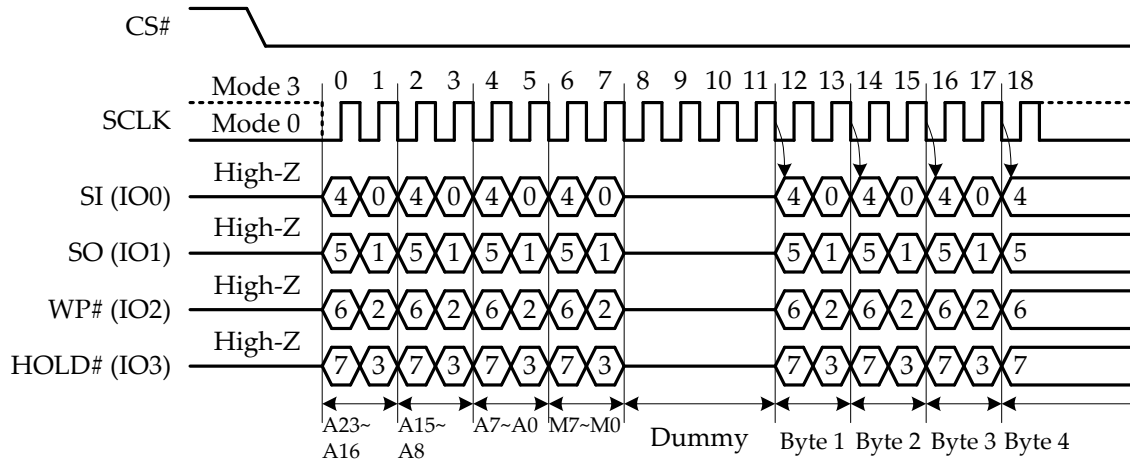
Figure 16: Quad I/O Fast Read (EBh) Command Sequence, (M5, M4) = (1, 0)

8.11.2. Quad I/O Fast Read with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Quad I/O Fast Read command can access a specific portion within a page by issuing "Set Burst with Wrap" (77h) command prior to EBh. The 77h command enables or disables the "Wrap Around" feature for the following EBh command by setting the W4, W5 and W6 bits.

The "Wrap Around" feature is reset by the following operations:

Power up;

Software Reset (66h + 99h) Command;

Another 77h command that resets W4, W5 and W6 bits.

This feature allows applications that use cache to quickly fetch data from a critical address and then fill the cache with a fixed length (8-, 16-, 32- or 64-byte) of data without issuing multiple read commands.

8.12. Quad I/O Word Fast Read (E7h)

E7h is similar to EBh command with the exception that the lowest address bit (A0) must be 0 and that there are only two dummy clocks. The first address can point to any location in the main array; after each byte is output, the address automatically increments to the next byte address.
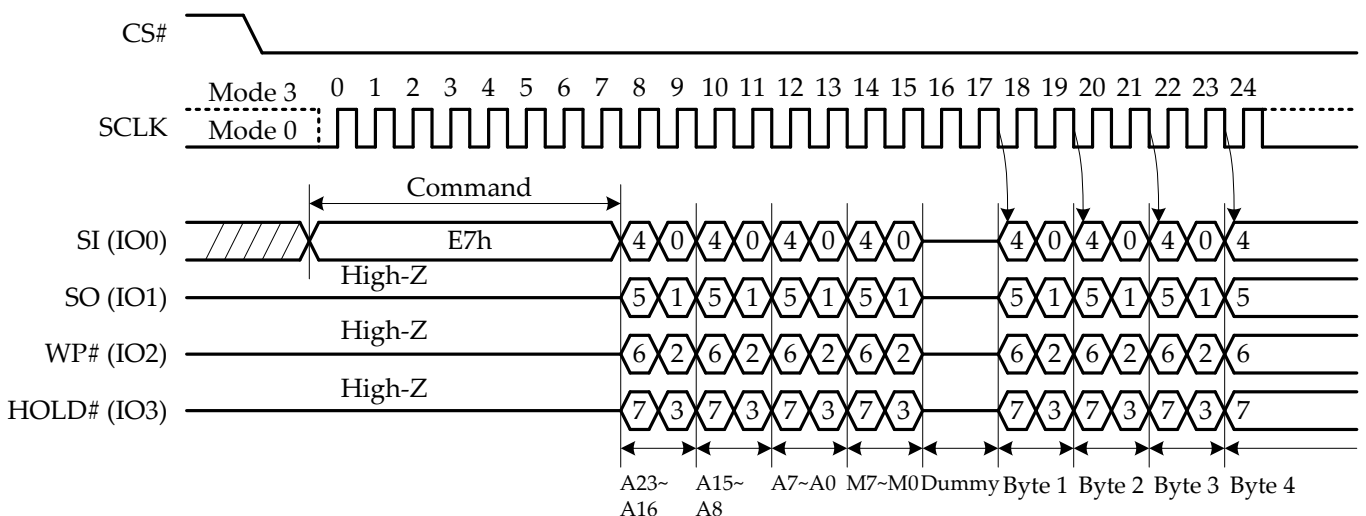
This command requires the QE bit to be set.

Figure 17: Quad I/O Word Fast Read (E7h) Command Sequence, (M5~M4) ≠ (1, 0)

8.12.1. Continuous Read Mode

The E7h command can further reduce command overhead using "Continuous Read Mode" bits M7~M0. If (M5~M4) is (1, 0), then the next operation after CE# goes high and then low remains in the state of Quad I/O Word Fast Read, and does not require the E7h opword; otherwise, the device just remains in normal mode.
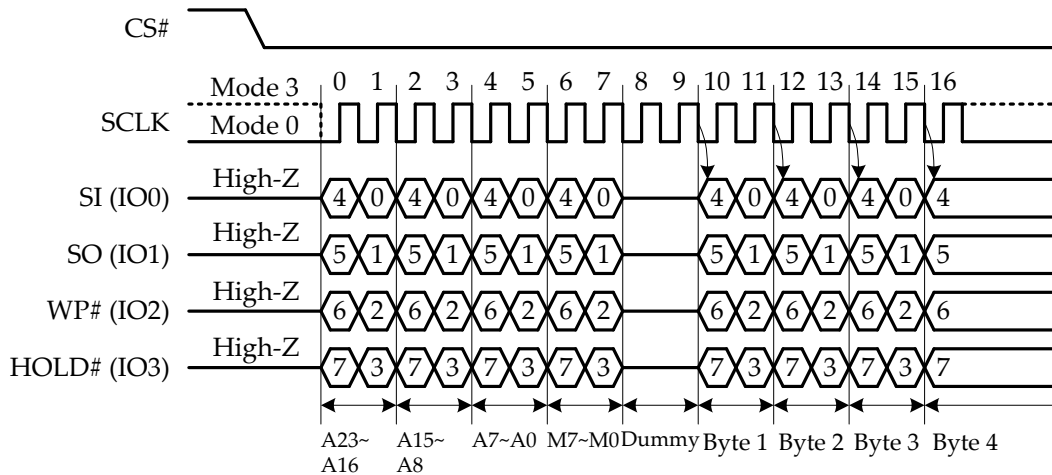

Figure 18: Quad I/O Word Fast Read (E7h) Command Sequence, (M5~M4) = (1, 0)

8.12.2. Quad I/O Word Fast Read with "8-, 16-, 32- or 64-Byte Wrap Around" in Standard SPI mode

The Quad I/O Word Fast Read (E7h) command can access a specific portion within a page by issuing "Set Burst with Wrap" (77h) command prior to E7h. The 77h command enables or disables the "Wrap Around" feature for the following E7h commands by setting the W4, W5 and W6 bits.
The "Wrap Around" feature is reset by the following operations:

Power up

Software Reset (66h + 99h) Command

Another 77h command that resets W4, W5 and W6 bits

This feature allows applications that use cache to quickly fetch data from a critical address and then fill the cache with a fixed length (8-, 16-, 32- or 64-byte) of data without issuing multiple read commands.

8.13. Set Burst with Wrap (77h)

The "Set Burst with Wrap" command 77h command allows three "Wrap Bits" W4 through W6 to be set. When 77h is used with EBh or E7h command, certain combinations of W4, W5 and W6 bits enable the EBh/E7h command to iteratively access a fixed length of 8-, 16-, 32- or 64-byte section within a 256-byte page.

The W4 bit enables or disables the "Wrap Around" operation. When W4 is 0, the Wrap Around mode is enabled and (W6, W5) specify the length of the wrap around section within a page. Once the W6~W4 bits are set, they apply to all upcoming EBh and E7h commands until the next power-up.

The W6~W4 bits are reset by:

Power up;

Software Reset (66h+99h) Command;

Another 77h command that resets W4, W5 and W6 bits.

Table 16: Wrap Bit Definition

W6, W5	W4=0		W4=1 (Default)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0, 0	Yes	8-byte	No	N/A

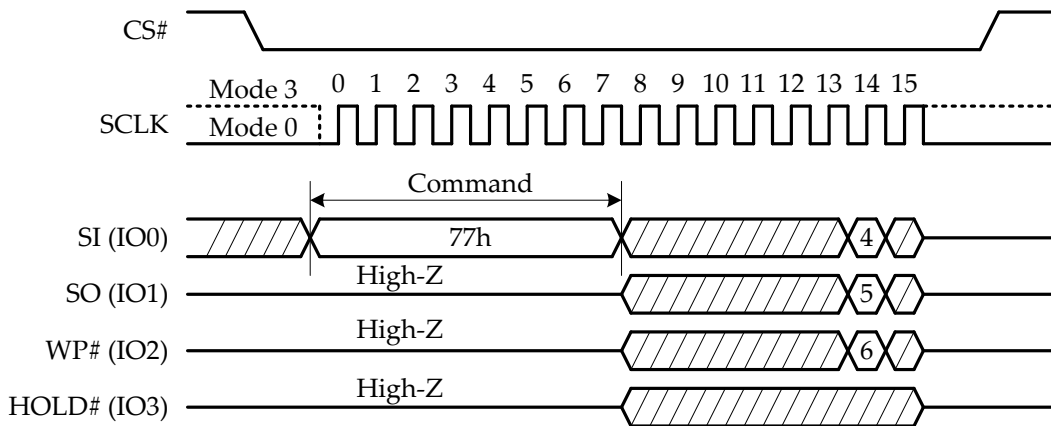| 0, 1 | Yes | 16-byte | No | N/A |
| 1, 0 | Yes | 32-byte | No | N/A |
| 1, 1 | Yes | 64-byte | No | N/A |

Figure 19: Set Burst with Wrap (77h) Command Sequence

8.14. Page Program (PP) (02h)

The PP command programs data to a specified location in the main memory array. The maximum amount of data to program in one PP operation is 256 bytes. WEL bit must be set to enable the device for programming operation. Attempting to program a memory location that has previously been programmed but not erased may corrupt the data.

The command sequence is as follows:

Drive CS# low --> Send in 02h opcode --> Send in three address bytes --> Send in data --> Drive CS# high.

Figure 20: Page Program (PP) (02h) Command Sequence

The address specified in the 02h command is the starting address of the program operation; this address can point to any location in the main memory array. The host may send in an arbitrary amount of data, however when the address points to the ending boundary of the current page, it automatically rolls back to the starting boundary of that page. Thus, all data bytes of a PP command fall within a single 256-byte page in the main array.

If more than 256 bytes of data are sent to the device, only the last 256 bytes take effect, and all previously latched data are discarded. If less than 256 data bytes are sent, they can be correctly programmed at the target addresses without affecting other bytes in the same page.

The CS# pin must be driven high exactly at a byte boundary, otherwise the command is ignored. After CS# is driven high, a self-timed Page Program cycle (t_PP) is initiated. While the Page Program cycle is in progress, it is recommended to continuously check the WIP bit in the Status Register. After the programming cycle is complete, the WEL bit is reset to 0.

A Page Program (PP) command applied to a page which is protected by Block Protect bits (BP4, BP3, BP2, BP1, and BP0) is not executed.

8.15. Quad Page Program (32h)

The 32h command uses IO0, IO1, IO2 and IO3 pins to program data to a specified location in the main memory array. The maximum amount of data to program in one Quad Page Program operation is 256 bytes. WEL bit must be set to enable the device for programming operation. Attempting to program a memory location that has previously been programmed but not erased may corrupt the data. QE bit must be set to use 32h command.

The command sequence is as follows:

Drive CS# low --> Send in 32h opcode --> Send in three address bytes --> Send in data, four bits per SCLK cycle --> Drive CS# high.
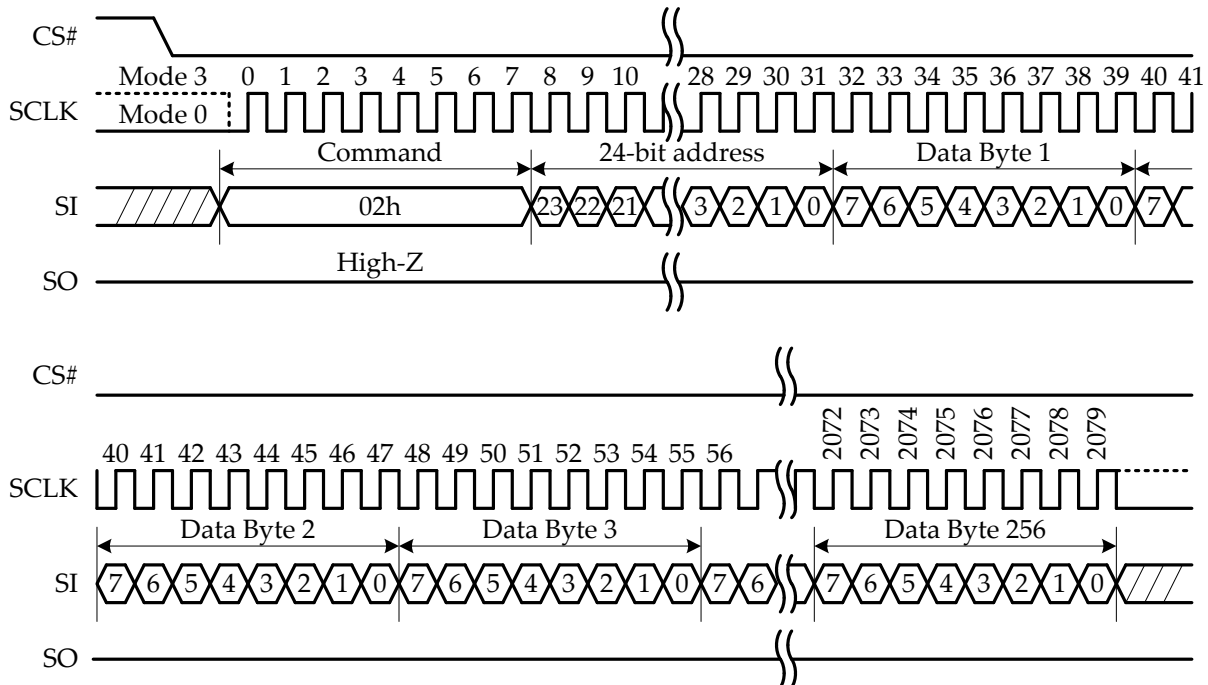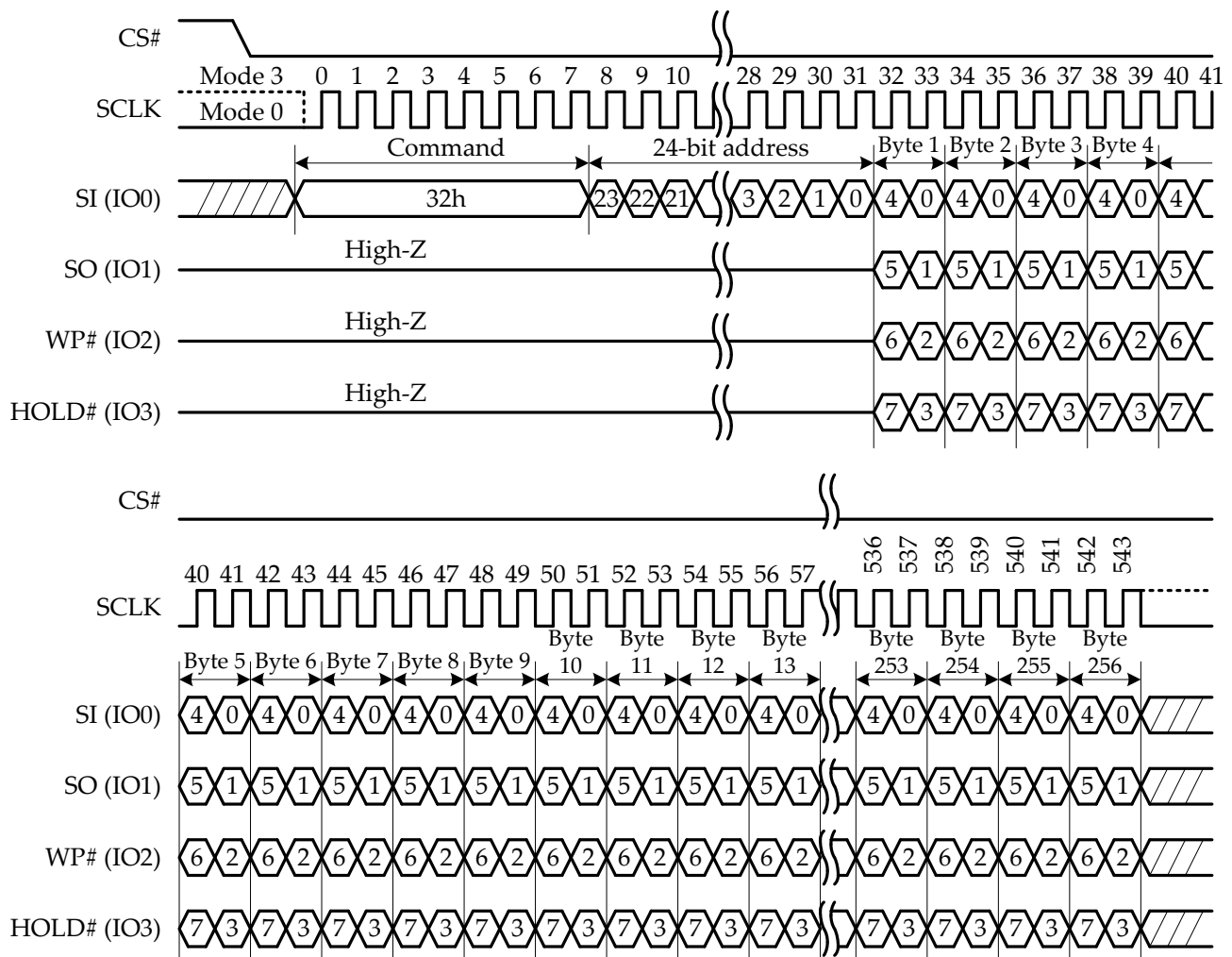

Figure 21: Quad Page Program (32h) Command Sequence

The address specified in the 32h command is the starting address of the program operation; this address can point to any location in the main memory array. The host may send in an arbitrary amount of data, however when the address points to the ending boundary of the current page, it automatically rolls back to the

starting boundary of that page. Thus, all data bytes of a 32h command fall within a single 256-byte page in the main array.

If more than 256 bytes of data are sent to the device, only the last 256 bytes take effect, and all previously latched data are discarded. If less than 256 data bytes are sent, they can be correctly programmed at the target addresses without affecting other bytes in the same page.

After CS# is driven high, a self-timed Quad Page Program cycle (tPP) is initiated. While the Quad Page Program cycle is in progress, it is recommended to continuously check the WIP bit in the Status Register. After the programming cycle is complete, the WEL bit is reset to 0.

A 32h command applied to a page which is protected by Block Protect bits (BP4, BP3, BP2, BP1, and BP0) is not executed.

8.16. Fast Page Program (FPP) (F2h)

The Fast Page Program command programs data to a specified location in the main memory array. The maximum amount of data to program in one operation is 256 bytes. WEL bit must be set to enable the device for programming operation. Attempting to program a memory location that has previously been programmed but not erased may corrupt the data.

The command sequence is as follows:

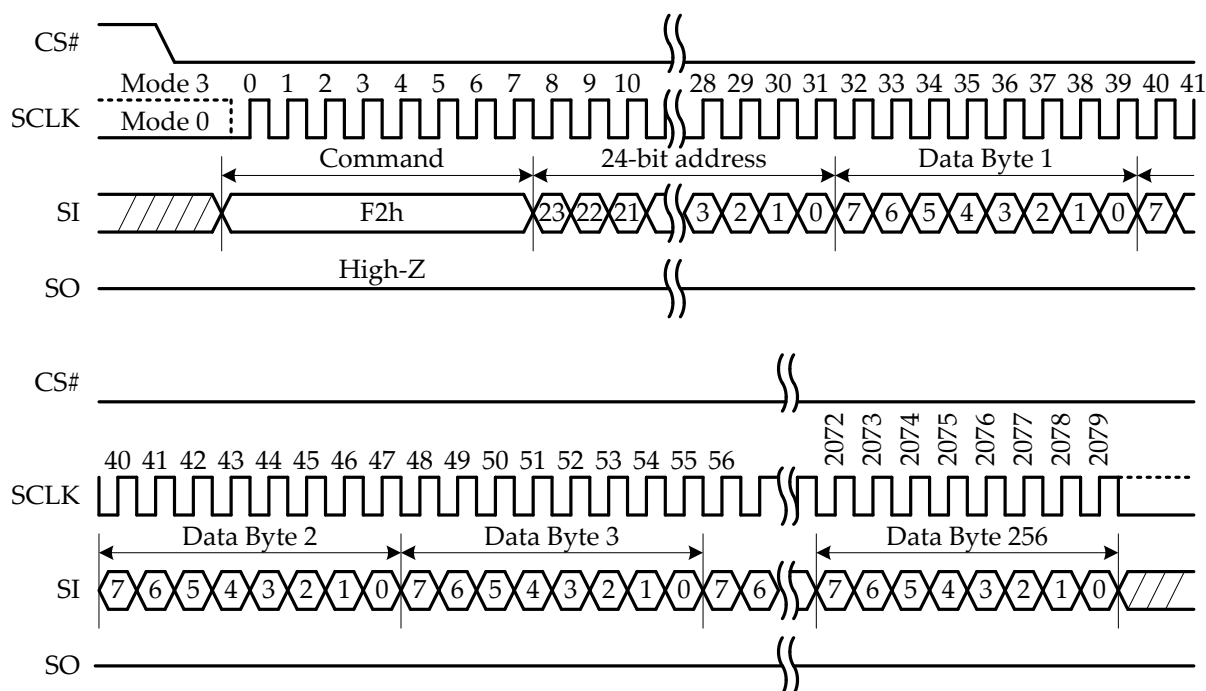Drive CS# low --> Send in F2h opcode --> Send in three address bytes --> Send in data --> Drive CS# high.

Figure 22: Fast Page Program (FPP) (F2h) Command Sequence

The address specified in F2h command is the starting address of the program operation; this address can point to any location in the main memory array. The host may send in an arbitrary amount of data, however when the address points to the ending boundary of the current page, it automatically rolls back to the starting boundary of that page. Thus, all data bytes of a Fast PP command fall within a single 256-byte page in the main array.

If more than 256 bytes of data are sent to the device, only the last 256 bytes take effect, and all previously latched data are discarded. If less than 256 data bytes are sent, they can be correctly programmed at the target addresses without affecting other bytes in the same page.

After CS# is driven high, a self-timed Page Program cycle (tPP) is initiated. While the Page Program cycle is in progress, it is recommended to continuously check the WIP bit in the Status Register. After the programming cycle is complete, the WEL bit is reset to 0.

A Fast Page Program command applied to a page which is protected by Block Protect bits (BP4, BP3, BP2, BP1, and BP0) is not executed.

8.17. Sector Erase (SE) (20h)

SE command erases the specified 4KB sector and sets all bytes in the target sector to FFh. WREN command is required to set WEL bit prior to an erase operation. Any address within the sector is a valid address for the SE command.

The command sequence is as follows:

Drive CS# low --> Send in 20h opcode --> Send 3 bytes of address on SI --> Drive CS# high.

The CS# pin must be driven high after the eighth bit of the 3-byte address input, otherwise the erase operation is not executed. After CS# is driven high, the device internally initiates a self-timed Sector Erase cycle (t_{SE}). It is recommended to poll WIP bit continuously while an SE operation is in progress. WIP is 1 during the self-timed Sector Erase cycle, and becomes 0 when it is complete. At some unspecified time before the erase cycle is complete, the WEL bit is reset.

A Sector Erase command applied to a sector which is protected by Block Protect bits (BP4, BP3, BP2, BP1, BP0) is not executed.

Figure 23: Sector Erase (SE) (20h) Command Sequence

8.18. 32KB Block Erase (BE) (52h)

32KB BE command erases the specified 32KB Block and sets all bytes in the target block to FFh. WREN command is required to set WEL bit prior to an erase operation. Any address within the 32KB block is a valid address for the BE command.

The command sequence is as follows:

Drive CS# low --> Send in 52h opcode --> Send 3 bytes of address on SI --> Drive CS# high.

The CS# pin must be driven high after the eighth bit of the 3-byte address input, otherwise the erase operation is not executed. After CS# is driven high, the device internally initiates a self-timed Block Erase cycle (t_{BE}). It is recommended to poll WIP bit continuously while a BE operation is in progress. WIP is 1 during the self-timed Block Erase cycle, and becomes 0 when it is complete. At some unspecified time before the erase cycle is complete, the WEL bit is reset.

A Block Erase command applied to a sector which is protected by Block Protect bits (BP4, BP3, BP2, BP1, BP0) is not executed.
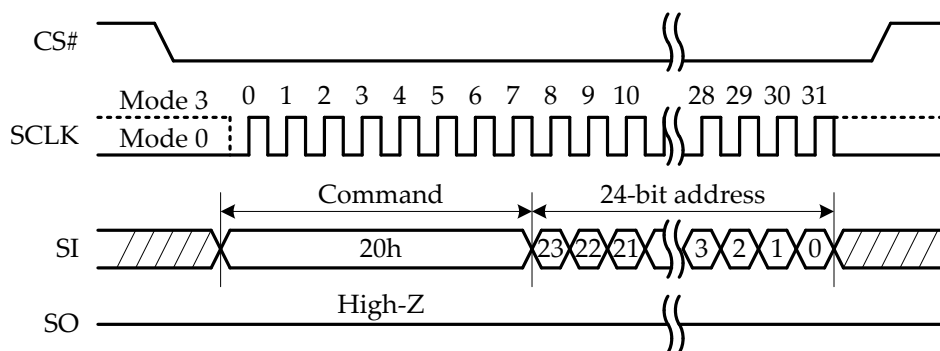
Figure 24: 32KB Block Erase (BE) (52h) Command Sequence

8.19. 64KB Block Erase (BE) (D8h)

64KB BE command erases the specified 64KB Block and sets all bytes in the target block to FFh. WREN command is required to set WEL bit prior to an erase operation. Any address within the 64KB block is a valid address for the BE command.

The command sequence is as follows:

Drive CS# low --> Send in D8h opcode --> Send 3 bytes of address on SI --> Drive CS# high.

The CS# pin must be driven high after the eighth bit of the 3-byte address input, otherwise the erase operation is not executed. After CS# is driven high, the device internally initiates a self-timed Block Erase cycle (t_{BE}). It is recommended to poll WIP bit continuously while a BE operation is in progress. WIP is 1 during the self-timed Block Erase cycle, and becomes 0 when it is complete. At some unspecified time before the erase cycle is complete, the WEL bit is reset.

A Block Erase command applied to a sector which is protected by Block Protect bits (BP4, BP3, BP2, BP1, BP0) is not executed.
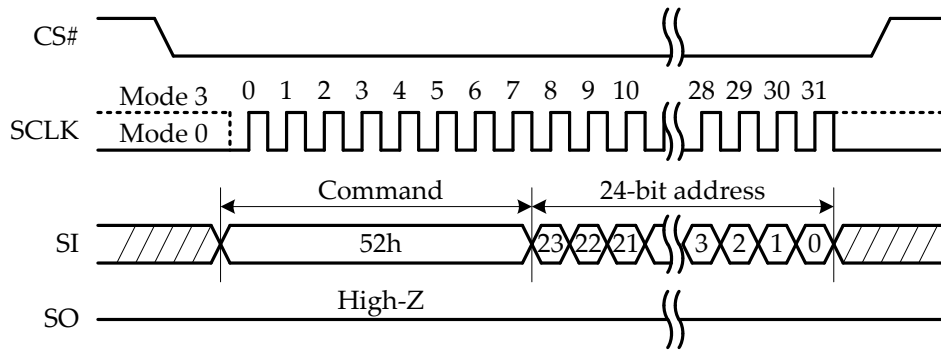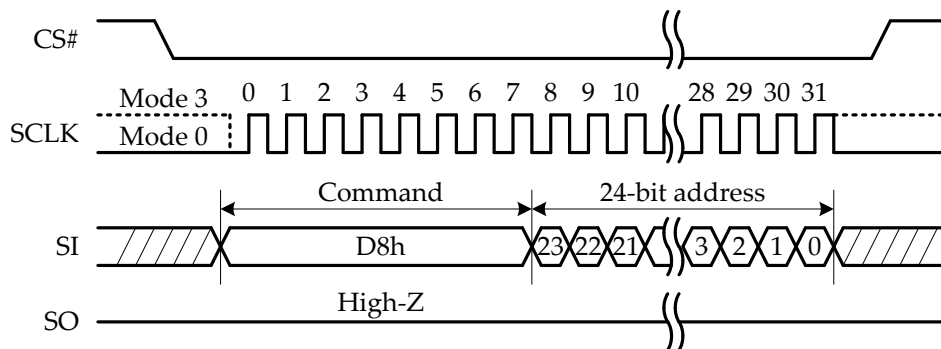

Figure 25: 64KB Block Erase (BE) (D8h) Command Sequence

8.20. Chip Erase (CE) (60h/C7h)

Chip Erase command erases the entire main memory array and sets all bytes in the array to FFh. WREN command is required to set WEL bit prior to an erase operation. The command sequence is as follows:

Drive CS# low --> Send in 60h or C7h opcode --> Drive CS# high.

The CS# pin must be driven high after the eighth bit of the command input, otherwise the erase operation is not executed. After CS# is driven high, the device internally initiates a self-timed Chip Erase cycle (t_{CE}). It is recommended to poll WIP bit continuously while a CE operation is in progress. WIP is 1 during the self-timed Chip Erase cycle, and becomes 0 when it is complete. At some unspecified time before the erase cycle is complete, the WEL bit is reset.

When a Chip Erase command is applied to a device, if any part of the main array is protected by Block Protect bits (BP4, BP3, BP2, BP1, BP0), then the command is not executed.
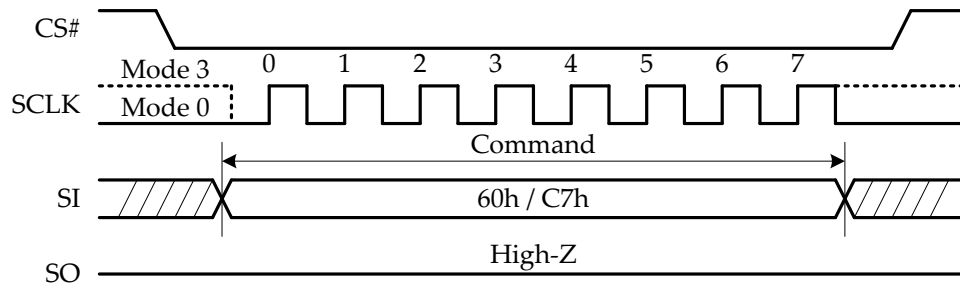
Figure 26: Chip Erase (CE) (60h/C7h) Command Sequence

8.21. Deep Power-Down (DP) (B9h)

DP command is the only way to bring the device into Deep Power-Down mode. In this mode, the supply current is reduced from standby current I_{CC1} to I_{CC2}. In this state, the device ignores all commands except "Release from Deep Power-Down and Read Device ID" (RDI) command. This command offers an extra software protection mechanism that protects the device from all WRSR, program or erase commands.

The command sequence is as follows:

Drive CS# low --> Send in B9h opcode --> Drive CS# high.

The CS# pin must be driven high after the eighth bit of the command input, otherwise the operation is not executed. As soon as CS# is driven high, the device first returns to standby mode if no internal WRSR, program or erase operation is in progress. After a delay of t_{DP}, the device enters Deep Power-Down Mode and current consumption is greatly reduced.

RDI command and power-down can release the device from Deep Power-Down mode and bring it back to standby mode. A DP command while WRSR, program or erase operation is in progress that can be ignored.
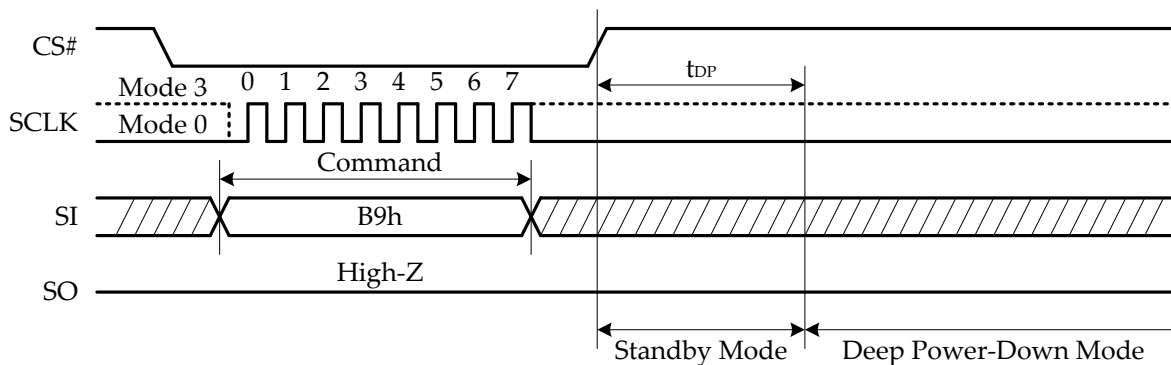

Figure 27: Deep Power-Down (DP) (B9h) Command Sequence

8.22. Release from Deep Power-Down or High Performance Mode and Read Device ID (RDI) (ABh)

8.22.1. Release from Deep Power-Down or High Performance Mode (ABh)

When issued alone and without any dummy cycles, the ABh command releases the device from Deep Power-Down state or High Performance Mode.

If the device is previously in Deep Power-Down mode, then after CS# transitions high, it takes t_{RES1} before the device resumes normal operation and other commands are accepted. The CS# pin must remain high during t_{RES1}; if the device is not previously in Deep Power-Down mode, then the transition to normal operation is immediate after CS# is deasserted.

If the ABh command is issued while a WRSR, program or erase operation is in progress, then the command is ignored.
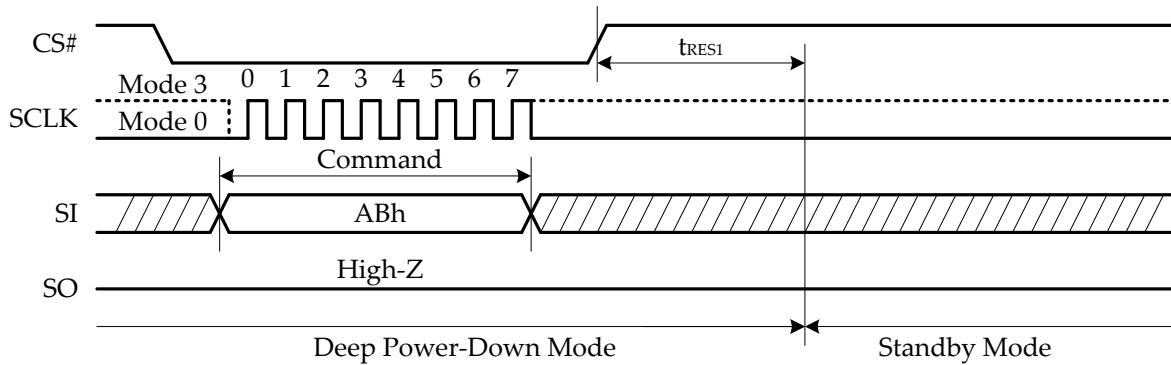
Figure 28: Release from Deep Power-Down or High Performance Mode (ABh) Command Sequence

8.22.2. Release from Deep Power-Down or High Performance Mode, And Read Device ID (RDI) (ABh)

If the device is previously in deep power-down mode, ABh can release the device from Deep Power-Down mode and obtain Device ID. The opcode is followed by three dummy bytes and the Device ID output byte. After CS# transitions high, it must remain high for at least tRES2 before the device returns to normal operation and other commands can be accepted.

If the ABh command is issued while a WRSR, program or erase operation is in progress, then the command is ignored.
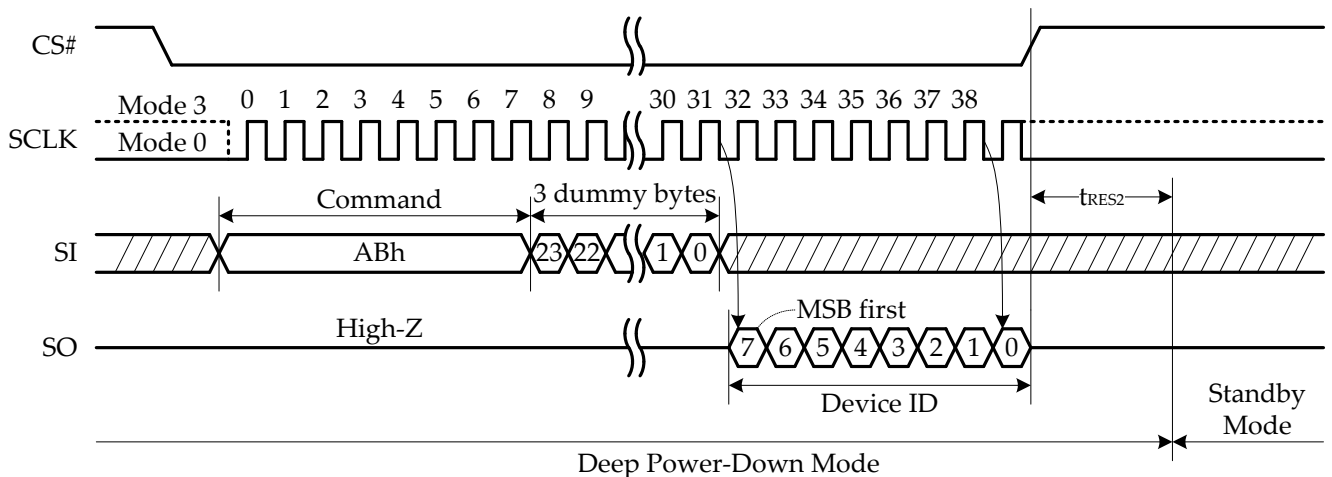

Figure 29: Release Deep Power-Down and Read Device ID (ABh) Command Sequence

8.22.3. Read Device ID (ABh)

If the device is not previously in deep power-down mode, ABh command can read Device ID. The opcode is followed by three dummy bytes and the Device ID output byte. After CS# transitions high, the device returns to standby mode immediately.
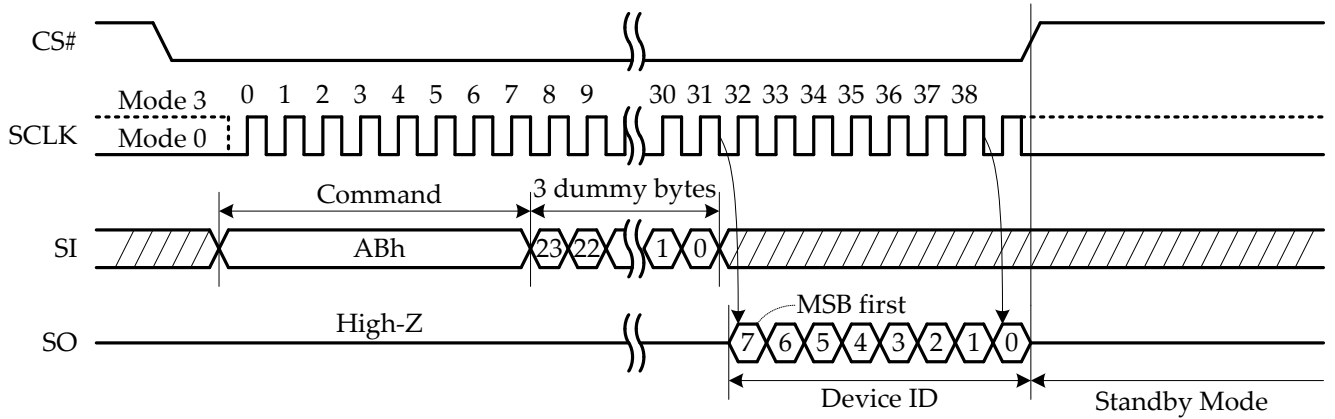
Figure 30: Read Device ID (ABh) Command Sequence

8.23. Read Unique ID (4Bh)

The Read Unique ID command accesses a factory-set read-only 128-bit number which is unique to each NM25Q16A device. The ID number can be used in conjunction with user software methods to help prevent illegal copying or cloning of a system. The command sequence is as follows:

Drive CS# pin low --> Shift in the 4Bh opcode --> Four bytes of dummy clocks --> Shift out the 128-Bit ID.

Data is shifted out on the falling edge of SCLK.
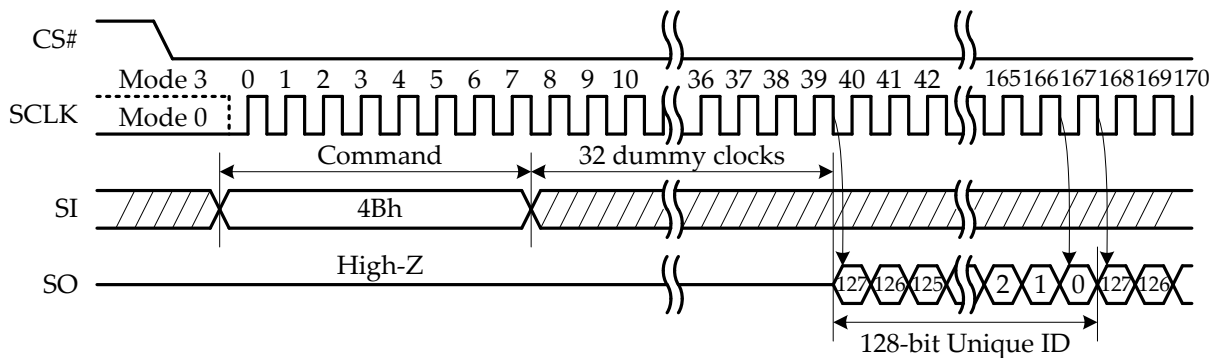
Figure 31: Read Unique ID (4Bh) Command Sequence

8.24. Read Manufacture ID / Device ID (REMS) (90h)

The 90h command provides both JEDEC assigned Manufacturer ID and Device ID. A 24-bit address is required following the 90h opcode. If address bit A0 is 0, then Manufacture ID is read out first; otherwise if A0 is 1, then Device ID is output first.

The command sequence is:

Drive CS# pin low --> Shift in 90h opcode --> Three bytes of address --> Shift out IDs.

Data is shifted out on SCLK falling edge. As long as CS# is low, the two IDs are repetitively output in turns.

Figure 32: Read Manufacture ID / Device ID (REMS) (90h) Command Sequence

8.25. Dual I/O Read Manufacture ID / Device ID (92h)

The 92h command outputs Manufacture ID and Device ID. A 24-bit address and 8 mode bits are required following the 92h opcode. If address bit A0 is 0, then Manufacture ID is output first; otherwise if A0 is 1, then Device ID is output first. The mode bits in 92h command do not bring the device into continuous read mode.

The command sequence is:

Drive CS# pin low --> Shift in 92h opcode --> Three bytes of Address and one byte of Mode bits on IO0 and IO1 --> Shift out ID data on IO0 and IO1.

Data is shifted out on SCLK falling edge. As long as CS# is low, the two IDs are repetitively output in turns.

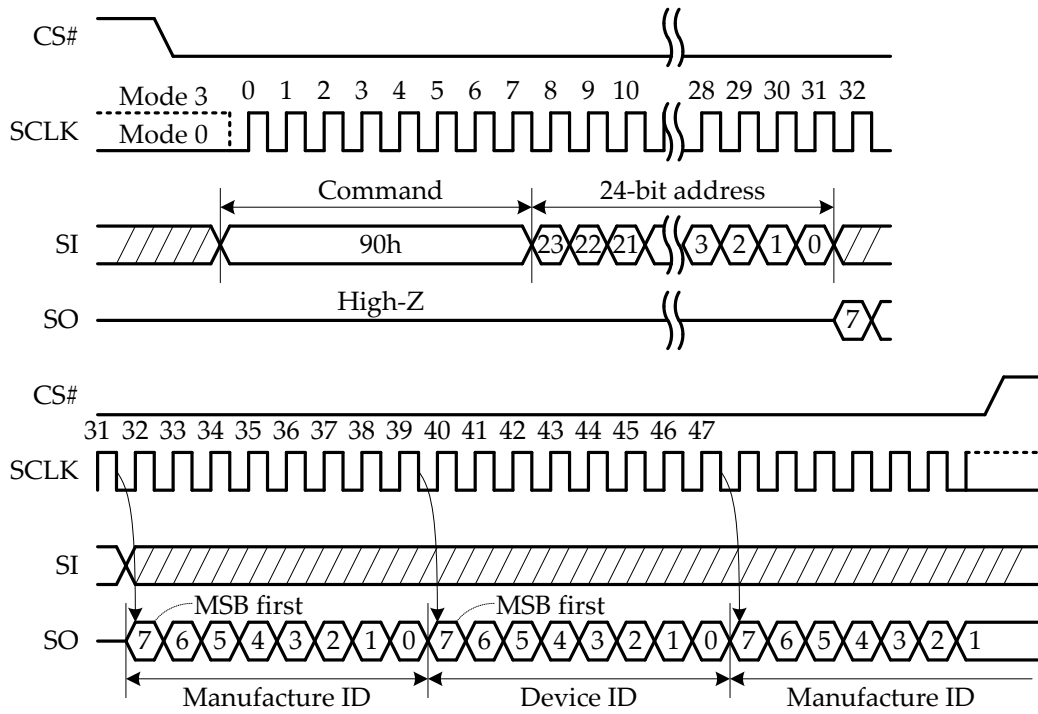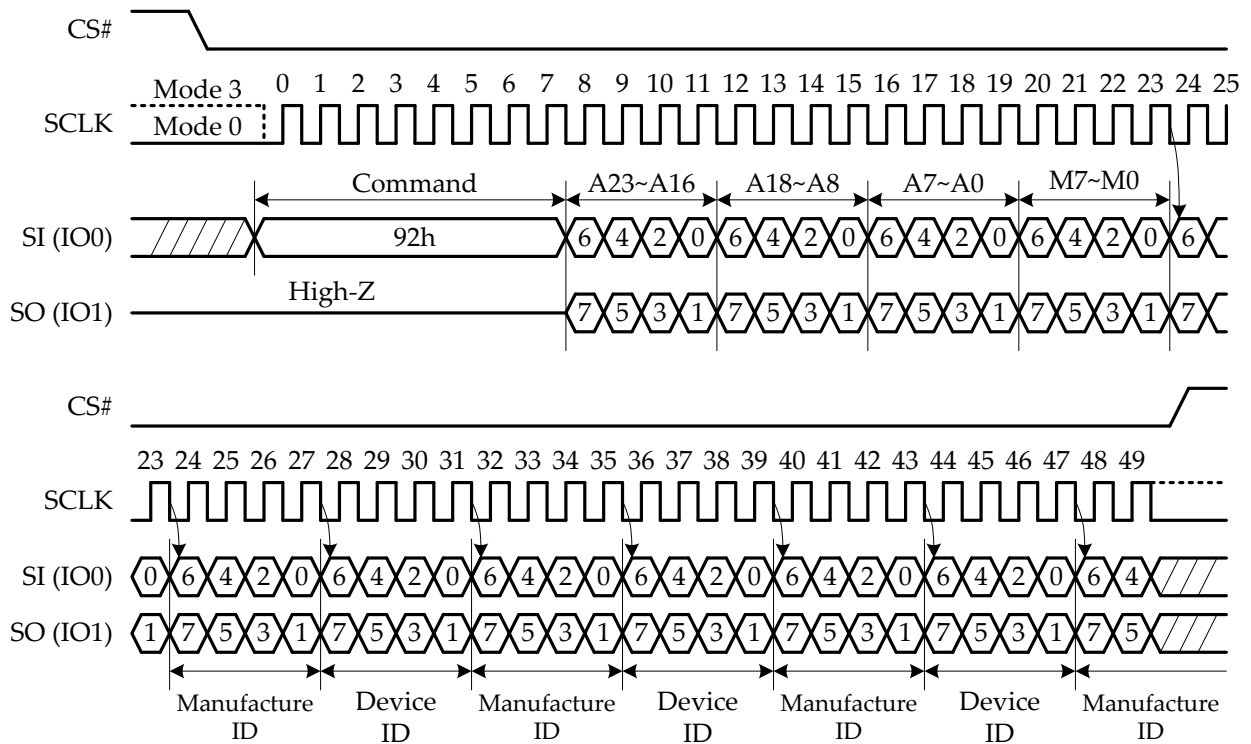**Figure 33: Dual I/O Read Manufacture ID / Device ID (92h) Command Sequence**

8.26. Quad I/O Read Manufacture ID / Device ID (94h)

The 94h command outputs Manufacture ID and Device ID. A 24-bit address, 8 mode bits and four dummy clocks are required following the 94h opcode. If address bit A0 is 0, then Manufacture ID is output first; otherwise if A0 is 1, then Device ID is output first. The mode bits in 94h command do not bring the device into continuous read mode. The QE bit should be set before the 94h command is issued.

The command sequence is:

Drive CS# pin low --> Shift in 94h opcode --> Three bytes of Address and one byte of Mode bits on IO0, IO1, IO2 and IO3 --> Four dummy clocks --> Shift out ID data on IO0, IO1, IO2 and IO3 pins.

Data is shifted out on SCLK falling edge. As long as CS# keeps low, the two IDs are repetitively output continuously.
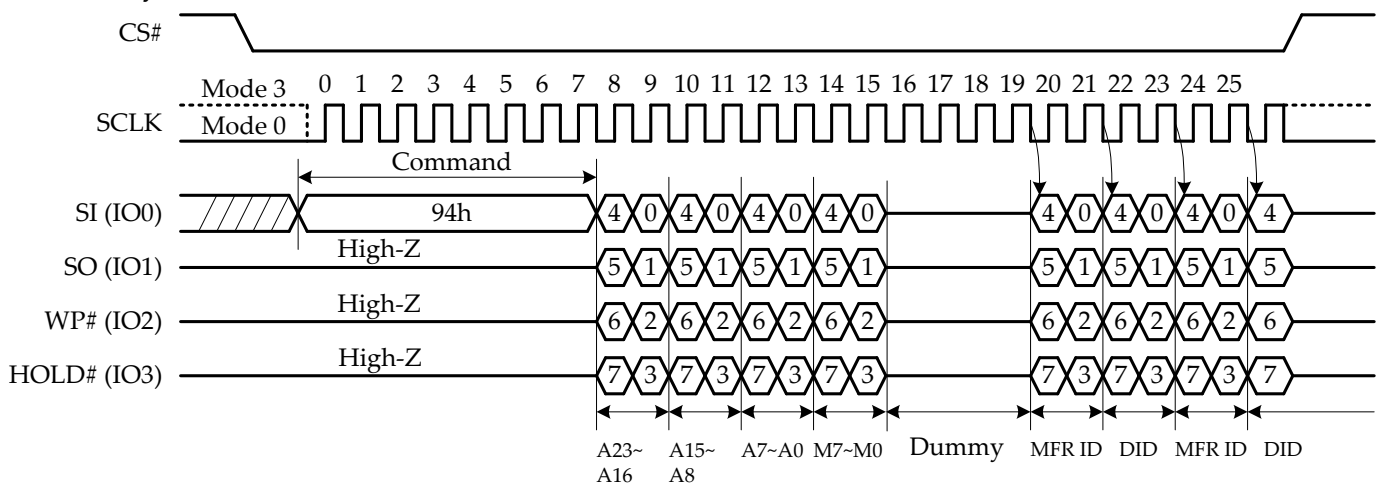

Figure 34: Quad I/O Read Manufacture ID / Device ID (94h) Command Sequence

8.27. Read Identification (RDID) (9Fh)

The 9Fh command outputs Manufacture ID, Memory Type and Memory Capacity ID codes. An RDID

command during WRSR, program or erase cycle is ignored.

The command sequence is:

Drive CS# pin low --> Shift in 9Fh opcode --> Shift out Manufacture ID data byte --> Shift out memory type data byte --> Shift out memory capacity data byte.

Data is shifted out on SCLK falling edge. The host may terminate the command by driving CS# high at any time during data output. As long as CS# keeps low, the three IDs will be repetitively output in turns.
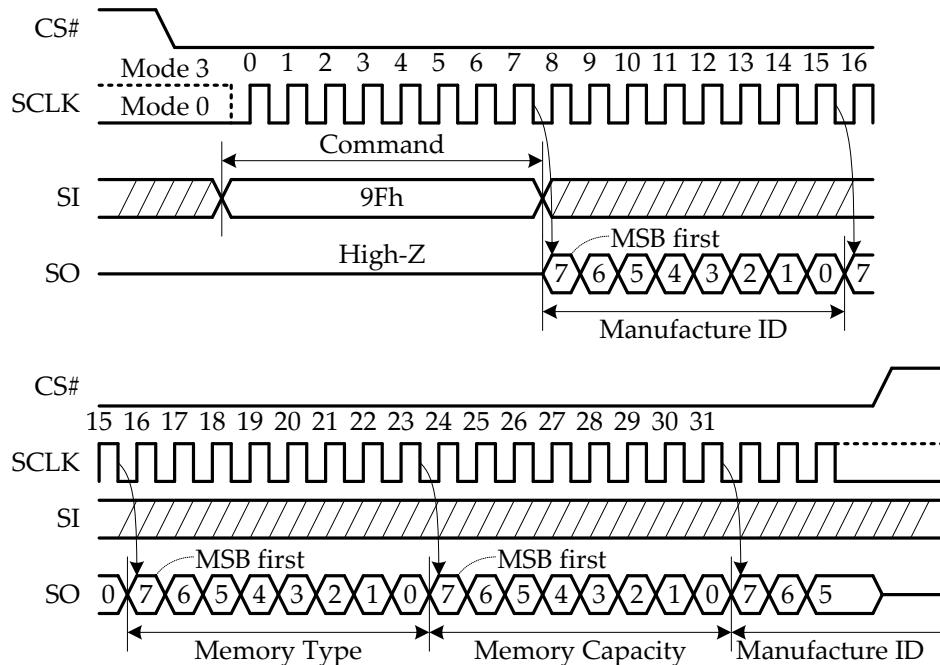
Figure 35: Read Identification (RDID) (9Fh) Command Sequence

8.28. High Performance Mode (HPM) (A3h)

The HPM command allows Dual and Quad I/O commands to operate at higher frequencies (see f_R and f_{C1}); it enables the pre-charging of internal charge pumps and makes the voltages readily available at the cost of higher power consumption.

The command sequence is:

Drive CS# pin low --> Shift in A3h opcode --> Shift in three dummy bytes --> Drive CS# high.

After HPM command is executed, the device assumes High Performance Mode after a delay of t_{HPM}. In this mode, the device consumes slightly higher standby current (I_{CC9}).

The Release from Deep Power-Down or High Performance Mode, And Read Device ID (RDI) command(ABH) releases the device from HPM mode and brings it to standby mode.

The Deep Power-Down command (B9H) releasees the device from HPM mode and brings it to deep power-down mode.

Figure 36: High Performance Mode (HPM) (A3h) Command Sequence

8.29. Program/Erase Suspend (PES) (75h)

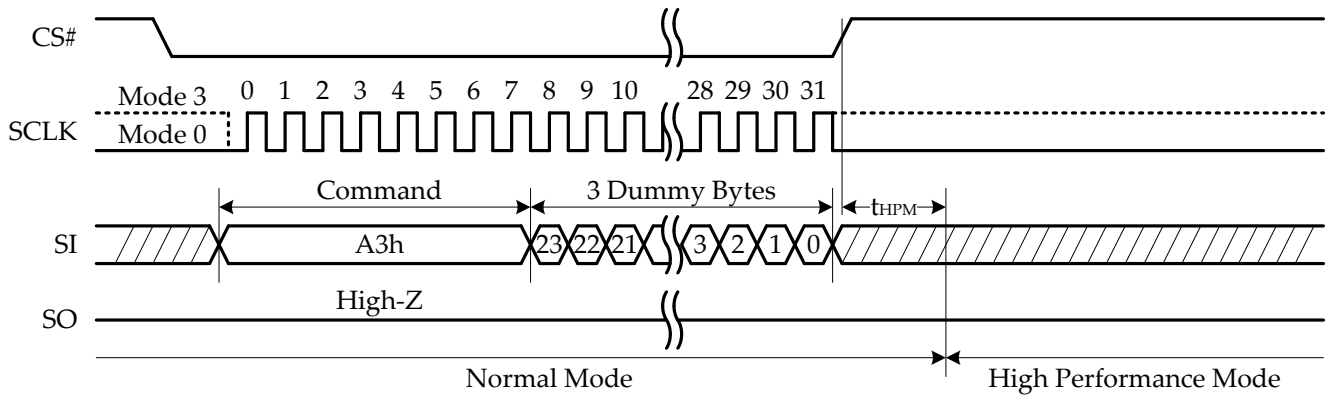The PES command is valid only during Page Program, Sector Erase or Block Erase commands. It allows the host to interrupt these operations and then read data from any other sector or block. A time duration of t_{SUS} is required for the PES command to take effect.

The WRSR (01h, 31h, 11h), Erase/Program Security Registers (44h, 42h), Erase (20h, 52h, D8h, 60h, C7h) and Page Program commands (02h, 32h) are not allowed during Program Suspend.

The WRSR (01h, 31h, 11h), Erase Security Registers (44h) and Erase commands (20h, 52h, D8h, 60h, C7h) are not allowed during Erase Suspend.

Immediately following PES command, the WIP bit is cleared from 1 to 0 within t_{SUS}, and the SUS2 or SUS1 bit is set from 0 to 1 depending on what operation is being suspended. Power down the device during suspension resets the device and releases it from suspend state.
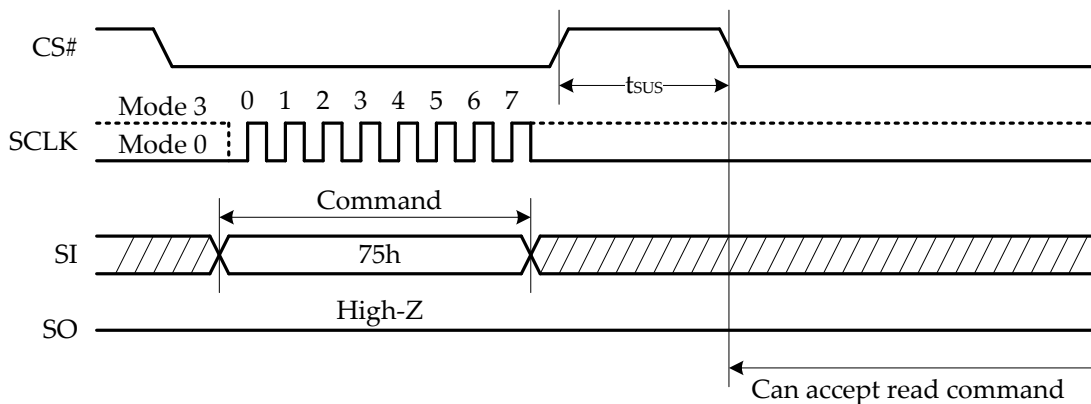
Figure 37: Program/Erase Suspend (PES) (75h) Command Sequence

8.30. Program/Erase Resume (PER) (7Ah)

While the device is in Program or Erase Suspension, the host may issue a PER command to bring the device out of Suspension and resume the Program or Erase operation previously suspended.

The PER command requires that either SUS1 or SUS2 bit = 1, and WIP = 0. After PER command is accepted, the SUS1 or SUS2 bit is cleared to 0, and WIP is set to 1 within 200ns to indicate the Program or Erase operation that is back in progress.

If no Program or Erase operation is in suspension, the PER command is ignored.

Figure 38: Program/Erase Resume (PER) (7Ah) Command Sequence

8.31. Erase Security Registers (44h)

The three 1024-byte Security Registers of the NM25Q16A device can be read, programmed or erased individually. The host may use Security Registers to store security or other important information separately from the main memory array.

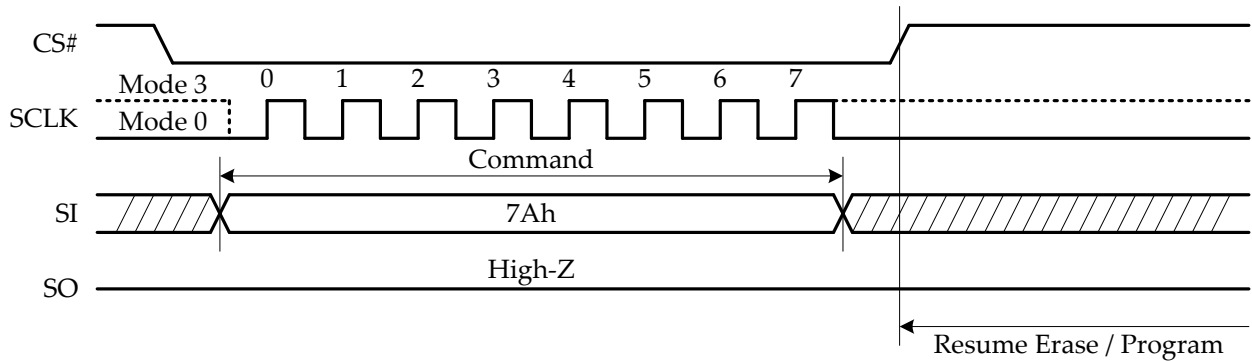Similar to Sector Erase and Block Erase commands, the 44h command requires that a WREN command be issued to set WEL bit = 1. The 44h command erases one of the three 1024-bit Security Registers; the command sequence is as follows:

Drive CS# low --> Shift in 44h command --> Send 3-byte address on SI pin --> Drive CS# high.

The address definition of 44h command is specified in *5.3 Security Register*. The CS# pin must be driven high after the last bit of address input, otherwise the command is ignored by the device.

After CS# transitions high, a self-timed Erase Security Registers cycle (t_{SE}) is initiated. The host may check the WIP bit while an erase cycle is in progress: the WIP bit is 1 during the self-timed Erase cycle, and is 0 when it is completed. At some unspecified time before the Erase cycle is completed, the WEL bit is reset.

Optionally, the Lock Bits (LB3, LB2, LB1) can each OTP protect a corresponding Security Register. Once protected, the Security Register is permanently protected against erase or program operations.
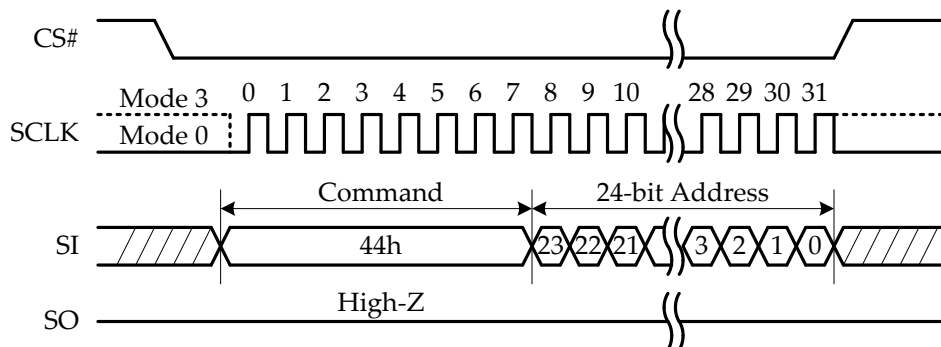
Figure 39: Erase Security Registers (44h) Command Sequence

8.32. Program Security Registers (42h)

The Program Security Register command programs data to a specified location in the Security Registers. WEL bit must be set to enable the device for programming operation. Attempting to program a memory location that has previously been programmed but not erased may corrupt the data.

The command sequence is as follows:

Drive CS# low --> Send in 42h opcode --> Send in 3-byte address -> Send in data -> Drive CS# high.

Figure 40: Program Security Registers (42h) Command Sequence

The address definition of 42h command is specified in *5.3 Security Register*, which specifies the starting address of the program operation; this address can point to any location in the security register. The host may send in an arbitrary amount of data, however when the address points to the ending boundary of the current page, it automatically rolls back to the starting boundary of that page. Thus, all data bytes of a Program Security Registers command fall within a single 256-byte page in the security register.
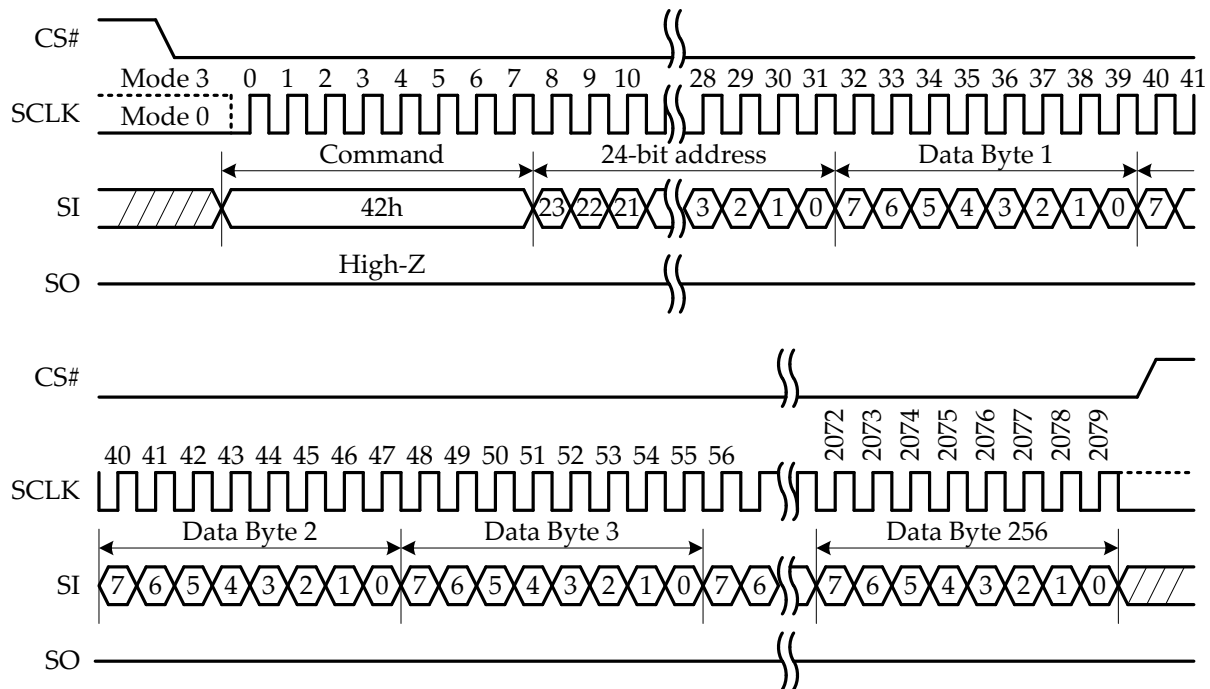
If more than 256 bytes of data are sent to the device, only the last 256 bytes take effect, and all previously latched data are discarded. If less than 256 data bytes are sent, they can be correctly programmed at the target addresses without affecting other bytes in the same page.

The CS# pin must be driven high exactly at a byte boundary, otherwise the command is ignored. After CS# is driven high, a self-timed Program Security Registers cycle (t_{PP}) is initiated. While the program cycle is in progress, it is recommended to check the WIP bit in the Status Register. After the programming cycle is complete, the WEL bit is reset to 0.

8.33. Read Security Registers (48h)

The Read Security Registers command is similar to Fast Read command. It outputs data bits at a maximum frequency of f_C. The first address can point to any location within a Security Register. The address automatically increments to the next byte address after each byte is shifted out. If the last byte address is reached, then the pointer will wrap back to the first byte address in the target Security Register.

The command sequence is as follows:

Drive CS# low --> Send in 48h opcode --> Send in 3-byte address -> One dummy byte --> Shift out read data on SO at SCLK falling edge.

The address definition of 48h command is specified in *5.3 Security Register*.
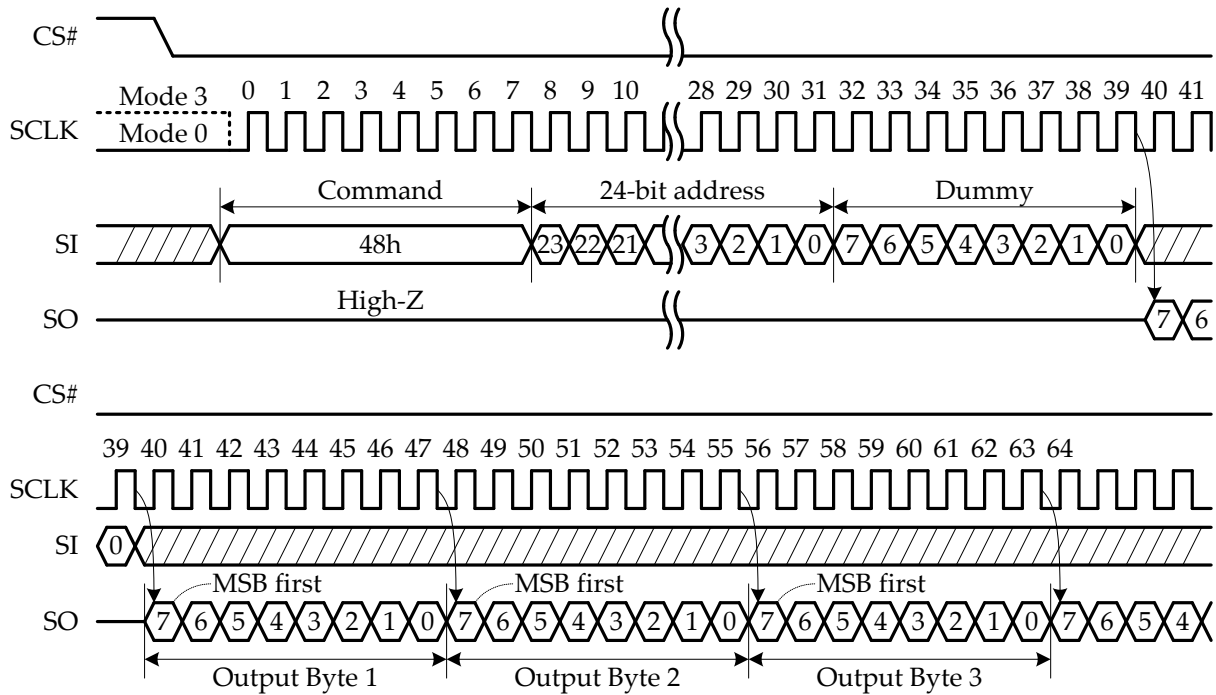
Figure 41: Read Security Registers (48h) Command Sequence

8.34. Enable Reset (66h) and Software Reset (99h)

The Software Reset command aborts all on-going internal operations, and brings the device back to its default power-on state. All volatile settings are lost, including Volatile Status Register bits, WEL, SUS1, SUS2, Continuous Read Mode bit setting (M7-M0) and Wrap Bit Setting (W6-W4). The command sequence is as follows:

Drive CS# low --> Send in 66h opcode --> Drive CS# high --> Drive CS# low --> Send in 99h opcode --> Drive CS# high.

After CS# goes high, the software reset process takes t_{RST_R}, during which no command is accepted.

Data corruption may occur if Software Reset command is used to interrupt an ongoing or suspended WRSR, program or erase operation. To prevent this, it is recommended to check WIP, SUS2 and SUS1 bits before issuing this command.
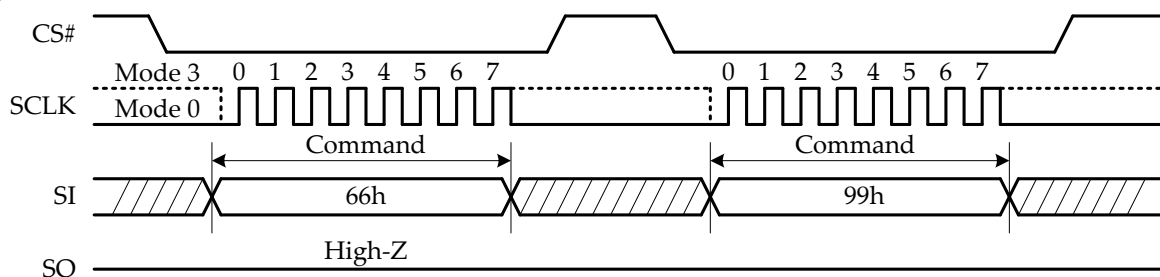
Figure 42: Enable Reset (66h) and Reset (99h) Command Sequence

8.35. Read Serial Flash Discoverable Parameter (5Ah)

The SFDP information is stored in a standard set of tables, which contain the functional and feature capabilities of the device. These tables can be interrogated by host to make adjustments needed to accommodate to different features from multiple vendors. SFDP is a JEDEC Standard (JESD216).

The address definition of 5Ah command is specified in *5.4 SFDP Register*.
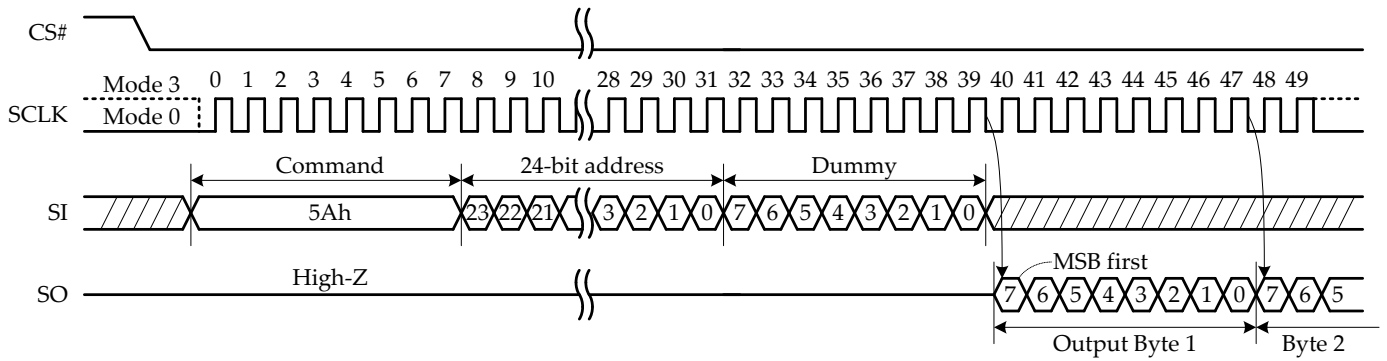
Figure 43: Read Serial Flash Discoverable Parameter (5Ah) Command Sequence

9. Electrical Characteristics

9.1. Power-On Timing
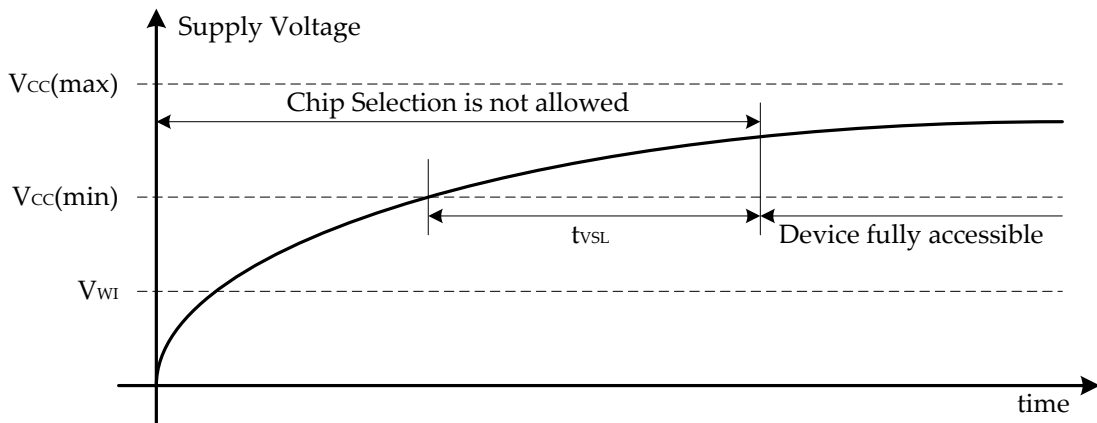
Figure 44: Power-On Timing Diagram

Table 17: Power-On Timing and Write Inhibit Threshold

Symbol	Comments	Min	Max	Unit
t_{VSL}	V_{CC}(min) to earliest CS# Low	5	----	ms
V_{WI}	Write Inhibit Voltage	1.5	2.5	V

9.2. Initial Delivery State

The device is delivered in the following status:

(1) The main memory array is erased; all bits are set to 1 (all bytes are FFh);

(2) The Status Register bits are all set to 0, except DRV0 bit (S21) is set to 1.

9.3. Absolute Maximum Ratings

Table 18: Absolute Maximum Ratings

Parameter	Value	Unit
Ambient Operating Temperature	-40 to 85	℃
Storage Temperature	-65 to 150	℃
Applied Input / Output Voltage	-0.6 to V_{CC}+0.4	V
Transient Input / Output Voltage (note: overshoot)	-2.0 to V_{CC}+2.0	V

V_{CC}	-0.6 to 4.0	V

Maximum Positive Overshoot Waveform   Maximum Negative Overshoot Waveform
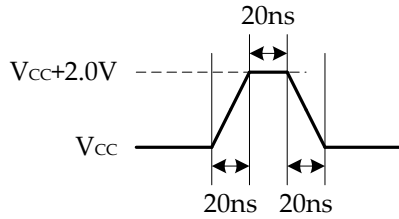
Figure 45: Maximum Positive / Negative Overshoot Timing Diagram

9.4. Capacitance Measurement Conditions

Table 19: Capacitance Measurement Conditions

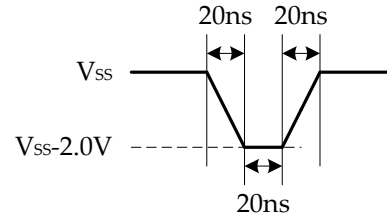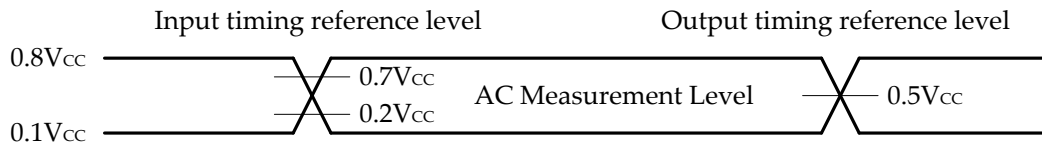| Symbol	Parameter	Min	Typ	Max	Unit	Conditions
C_{IN}	Input Capacitance	----	----	6	pF	V_{IN}=0V
C_{OUT}	Output Capacitance	----	----	8	pF	V_{OUT}=0V
C_L	Load Capacitance	30			pF	
	Input Rise And Fall time	----	----	5	Ns	
	Input Pulse Voltage	0.1V_{CC} to 0.8V_{CC}			V	
	Input Timing Reference Voltage	0.2V_{CC} to 0.7V_{CC}			V	
	Output Timing Reference Voltage	0.5V_{CC}			V	

Input timing reference level   Output timing reference level

Note: Input pulse rise and fall times both < 5ns.

Figure 46: Input Test Waveform and Measurement Level

9.5. DC Characteristics

Table 20: DC Characteristics at T= -40℃~85℃, V_{CC}=2.7~3.6V

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	----	----	----	±2	μA
I_{LO}	Output Leakage Current	----	----	----	±2	μA
I_{CC1}	Standby Current	CS#=V_{CC}, V_{IN}=V_{CC} or V_{SS}	----	5	10	μA
I_{CC2}	Deep Power-Down Current	CS#=V_{CC}, V_{IN}=V_{CC} or V_{SS}	----	1	5	μA
I_{CC3}	Operating Current (Read)	CLK=0.1V_{CC} / 0.9V_{CC} at 120MHz, Q=Open(*1,*2,*4 I/O)	----	15	20	mA
		CLK=0.1V_{CC} / 0.9V_{CC} at 80MHz, Q=Open(*1,*2,*4 I/O)	----	13	18	mA
I_{CC4}	Operating Current (PP)	CS#=V_{CC}	----	----	20	mA
I_{CC5}	Operating Current(WRSR)	CS#=V_{CC}	----	----	20	mA

I_{CC6}	Operating Current (SE)	CS#=V_{CC}	----	----	20	mA
I_{CC7}	Operating Current (BE)	CS#=V_{CC}	----	----	20	mA
I_{CC8}	Operating Current (CE)	CS#=V_{CC}	----	----	20	mA
I_{CC9}	High Performance Current	----	----	0.4	1.2	mA
V_{IL}	Input Low Voltage	----	----	----	$0.2V_{CC}$	V
V_{IH}	Input High Voltage	----	$0.7V_{CC}$	----	----	V
V_{OL}	Output Low Voltage	I_{OL} =100μA	----	----	0.2	V
V_{OH}	Output High Voltage	I_{OH} =-100μA	V_{CC}-0.2	----	----	V

9.6. AC Characteristics

Table 21: AC Characteristics at T= -40℃~85℃, V_{CC}=2.7~3.6V, C_L=30pf

Symbol	Parameter	Min	Typ	Max	Unit
F_C	Serial Clock Frequency For: Dual I/O (BBh), Dual Output (3Bh), Quad I/O (EBh), Quad Output (6Bh) (Dual I/O & Quad I/O Without High Performance Mode), on 3.0V-3.6V power supply	DC.	----	104	MHz
f_{C1}	Serial Clock Frequency For: Dual I/O (BBh), Dual Output (3Bh), Quad I/O (EBh), Quad Output (6Bh) (Dual I/O & Quad I/O Without High Performance Mode), on 2.7V-3.0V power supply	DC.	----	80	MHz
f_{C2}	Serial Clock Frequency For: Dual I/O (BBh), Dual Output (3Bh), Quad I/O (EBh), Quad Output (6Bh) (Dual I/O & Quad I/O With High Performance Mode), on 2.7V-3.6V power supply	DC.	----	120	MHz
f_{C3}	Serial Clock Frequency For: Fast Read (0Bh) (with/without High Performance Mode), on 2.7V-3.6V power supply	DC.	----	120	MHz
f_R	Serial Clock Frequency For: Read (03h), Read Status Register (05h, 15h, 35h), Read Device ID (ABh, 90h, 92h, 94h, 9Fh)	DC.	----	80	MHz
t_{CLH}	Serial Clock High Time	3.5	----	----	ns
t_{CLL}	Serial Clock Low Time	3.5	----	----	ns
t_{CLCH}	Serial Clock Rise Time (Slew Rate)	0.1	----	----	V/ns
t_{CHCL}	Serial Clock Fall Time (Slew Rate)	0.1	----	----	V/ns
t_{SLCH}	CS# Active Setup Time	5	----	----	ns
t_{CHSH}	CS# Active Hold Time	5	----	----	ns
t_{SHCH}	CS# Not Active Setup Time	5	----	----	ns
t_{CHSL}	CS# Not Active Hold Time	5	----	----	ns
t_{SHSL}	CS# High Time（read/write）	20	----	----	ns
t_{SHQZ}	Output Disable Time	----	----	6	ns
t_{CLQX}	Output Hold Time	1.2	----	----	ns
t_{DVCH}	Data In Setup Time	2	----	----	ns
t_{CHDX}	Data In Hold Time	2	----	----	ns
t_{HLCH}	HOLD# Low Setup Time (relative to Clock)	5	----	----	ns

t_{HHCH}	HOLD# High Setup Time (relative to Clock)	5	----	----	ns
t_{CHHL}	HOLD# High Hold Time (relative to Clock)	5	----	----	ns
t_{CHHH}	HOLD# Low Hold Time (relative to Clock)	5	----	----	ns
t_{HLQZ}	HOLD# Low To High-Z Output	----	----	6	ns
t_{HHQX}	HOLD# High To Low-Z Output	----	----	6	ns
t_{CLQV}	Clock Low To Output Valid	----	----	7	ns
t_{WHSL}	Write Protect Setup Time Before CS# Low	20	----	----	ns
t_{SHWL}	Write Protect Hold Time After CS# High	100	----	----	ns
t_{DP}	CS# High To Deep Power-Down Mode	----	----	20	μs
t_{RES1}	CS# High To Standby Mode Without Electronic Signature Read	----	----	20	μs
t_{RES2}	CS# High To Standby Mode With Electronic Signature Read	----	----	20	μs
t_{HPM}	CS# High To High Performance Mode	----	----	20	μs
t_{SUS}	CS# High To Next Command After Suspend	----	----	20	μs
t_{RST_R}	CS# High To Next Command After Reset (from read)	----	----	20	μs
t_{RST_P}	CS# High To Next Command After Reset (from program)	----	----	20	μs
t_{RST_E}	CS# High To Next Command After Reset (from erase)	----	----	12	ms
t_W	Write Status Register Cycle Time	----	5	30	ms
t_{PP}	Page Programming Time	----	0.6	2.4	ms
t_{SE}	Sector Erase Time(4K Bytes)	----	50	200/300[1]	ms
t_{BE1}	Block Erase Time(32K Bytes)	----	0.15	0.8/1.6[2]	s
t_{BE2}	Block Erase Time(64K Bytes)	----	0.20	1.2/2.0[3]	s
t_{CE}	Chip Erase Time(NM25Q16A)	----	8	60	s

Notes:

1. For 4KB Sector Erase, tSE max value is 200ms for ≤50K cycles, 300ms for >50K & ≤100K cycles.
2. For 32KB Block Erase, tBE1 max value is 0.8s for ≤50K cycles, 1.6s for >50K & ≤100K cycles.
3. For 64KB Block Erase, tBE2 max value is 1.2s for ≤50K cycles, 2.0s for >50K & ≤100K cycles.

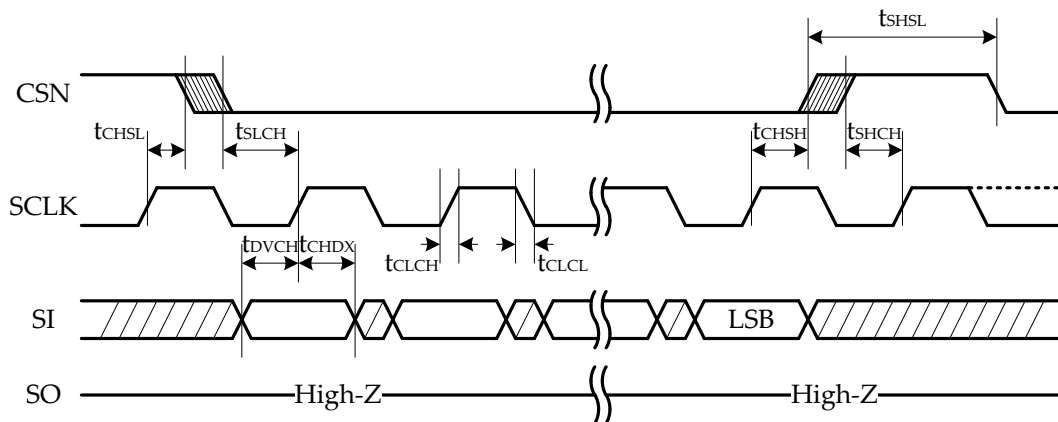## 9.6.1. Serial Input Timing Diagram

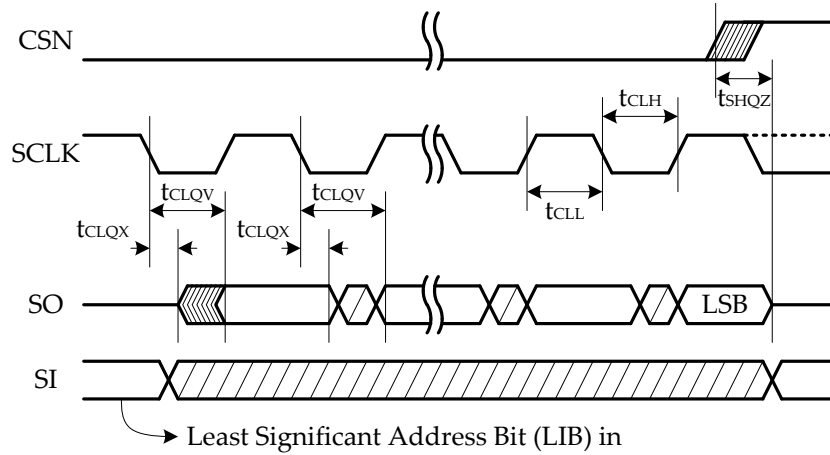**Figure 47: Serial Input Timing Diagram**

9.6.2. Serial Output Timing Diagram

Figure 48: Serial Output Timing Diagram

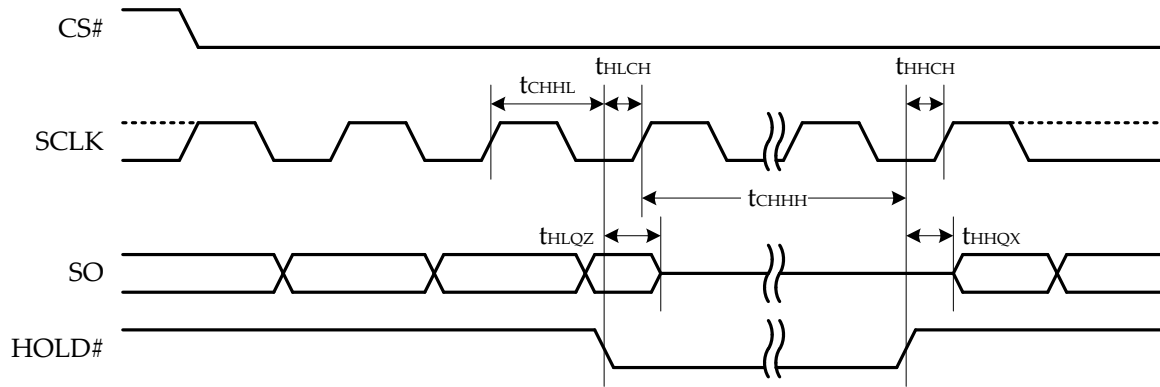## 9.6.3. Hold Timing Diagram

Figure 49: Hold Timing Diagram

9.7. Quality and Reliability Characteristics

Table 22: Quality and Reliability Characteristics

Symbol	Description	Min	Typ	Max	Units
T_{DR}	Data retention	----	20	----	Years
N_{PE}	Program/erase cycles (Endurance)	100,000	----	----	Cycles

10.   Ordering Information

NM   25   Q   16   A   X   X   X   X

Manufacturer
NM: NeuMem

Product Family
25: SPI NOR Flash
29: Parallel NOR Flash

Product Series
Q: 3.3V,4KB Uniform Sector
LQ: 1.8V,4KB Uniform Sector

Density
32: 32Mbit
64: 64Mbit
128: 128Mbit
256: 256Mbit
512: 512Mbit
01G: 1Gbit

Product Version
A: Version A
B: Version B
C: Version C

Package Type
B: FBGA-24
D: DIP8 300mil
F: FBGA-63
O:SOP8 150mil
P: SOP16 300mil
Q: WSON8 (6*5mm)
S: SOP8 208mil
U: USON8 (4*4mm, 0.45mm thickness)
W: Wafer
Y: WSON8 (8*6mm)
Z: TFBGA24 (6*4 Ball Array)

Temperature Range
C:Commercial (0°C to +70°C)
I: Industrial (-40°C to +85°C)
J: Industrial Plus (-40°C to +105°C)
A: Automotive (-40°C to +125°C)

Green Code
G: Pb Free & Halogen Free Green Package

Packing Type
T or no mark: Tube
Y: Tray
R: Tape & Reel

Figure 50: Device Ordering Information
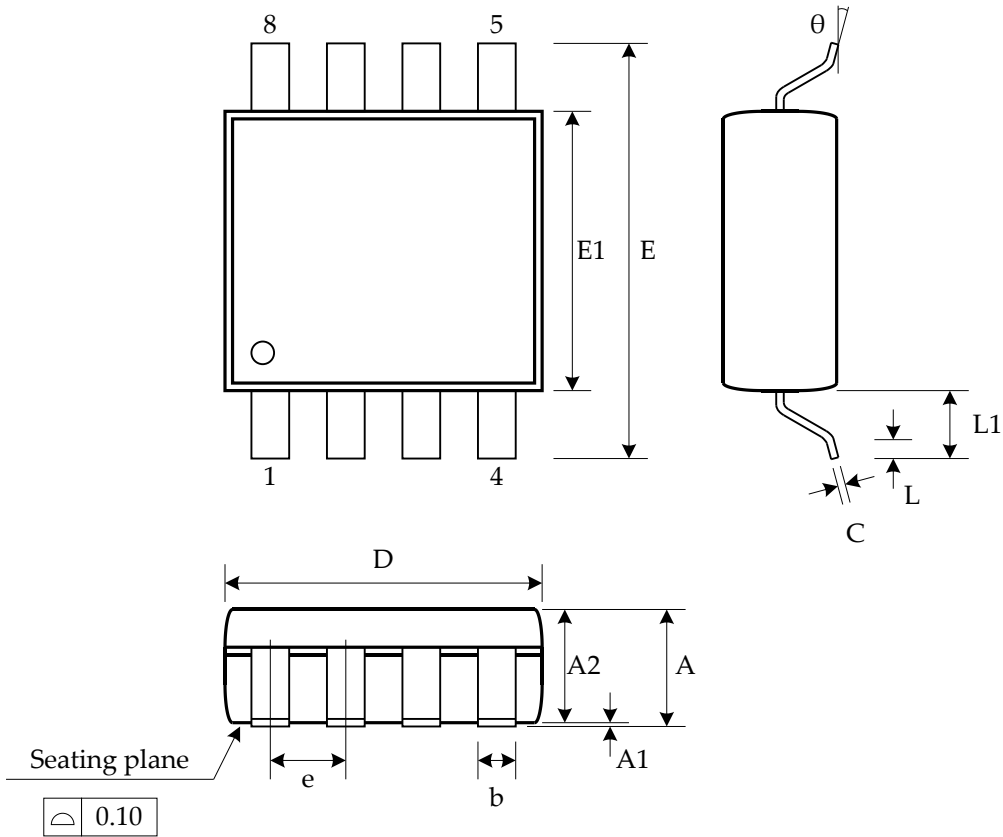
11.   Package Information

11.1. SOP8 (208mil)

Figure 51: SOP8(208mil) Package

Table 23: The Package Dimensions of SOP8(208mil)

Symbol		A	A1	A2	b	C	D	E	E1	e	L	L1	θ
Unit													
mm	MIN.		0.05	1.70	0.31	0.18	5.13	7.70	5.18		0.50	1.20	0
	NOM.		0.15	1.80	0.41	0.21	5.23	7.90	5.28	1.27 BSC	0.67	1.31	5
	MAX.	2.16	0.25	1.91	0.51	0.25	5.33	8.10	5.38		0.85	1.41	8
Inch	MIN.		0.002	0.067	0.012	0.007	0.202	0.303	0.204		0.020	0.048	0
	NOM.		0.006	0.071	0.016	0.008	0.206	0.311	0.208	0.050 BSC	0.026	0.052	5
	MAX.	0.085	0.010	0.075	0.020	0.010	0.210	0.319	0.212		0.033	0.056	8

Notes:

1. Package length and width do not include mold flash.

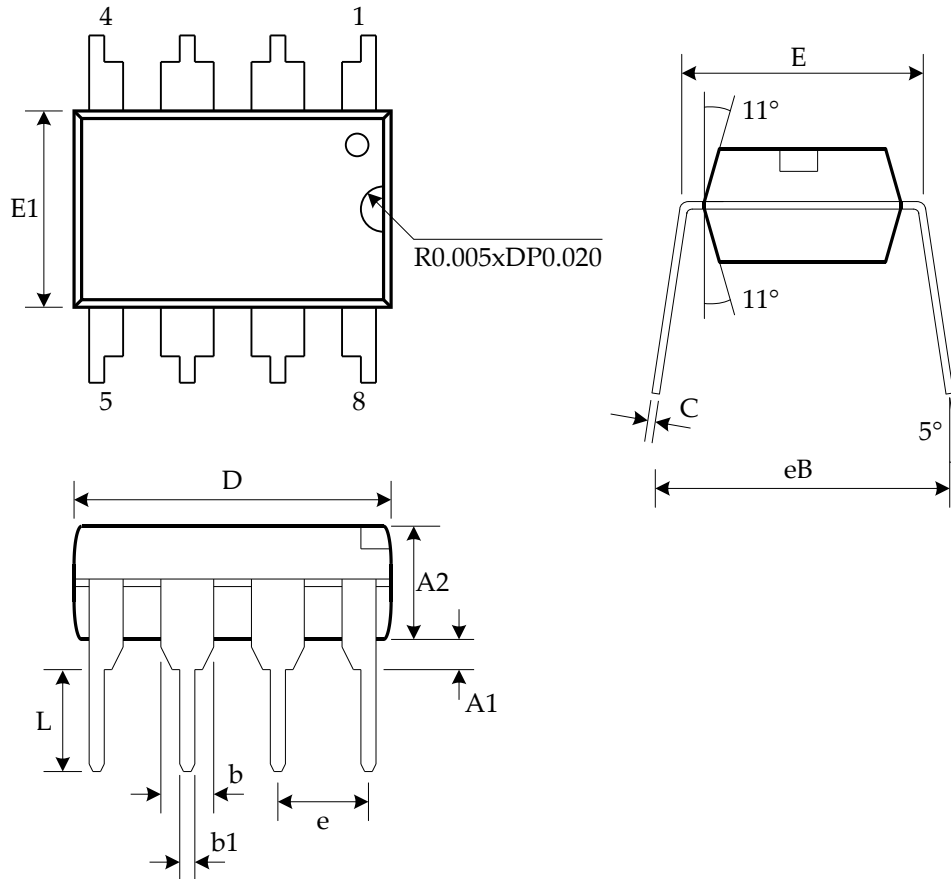2. Seating plane: Max. 0.10mm.

11.2. DIP8 (300mil)

Figure 52: DIP8(300mil) Package

Table 24: The Package Dimensions of DIP8(300mil)

Symbol Unit		A1	A2	b	b1	C	D	E	E1	e	eB	L
mm	MIN.	0.38	3.00	1.27	0.38	0.20	9.05	7.62	6.12		7.62	3.04
	NOM.	0.72	3.25	1.46	0.46	0.28	9.32	7.94	6.38	2.54	8.49	3.30
	MAX.	1.05	3.50	1.65	0.54	0.34	9.59	8.26	6.64		9.35	3.56
Inch	MIN.	0.015	0.118	0.050	0.015	0.008	0.356	0.300	0.242		0.333	0.120
	NOM.	0.028	0.128	0.058	0.018	0.011	0.367	0.313	0.252	0.100	0.345	0.130
	MAX.	0.041	0.138	0.065	0.021	0.014	0.378	0.326	0.262		0.357	0.140

Notes:

Package length and width do not include mold flash.

11.3. WSON8 (6*5mm)

Top View

Side View

Bottom View
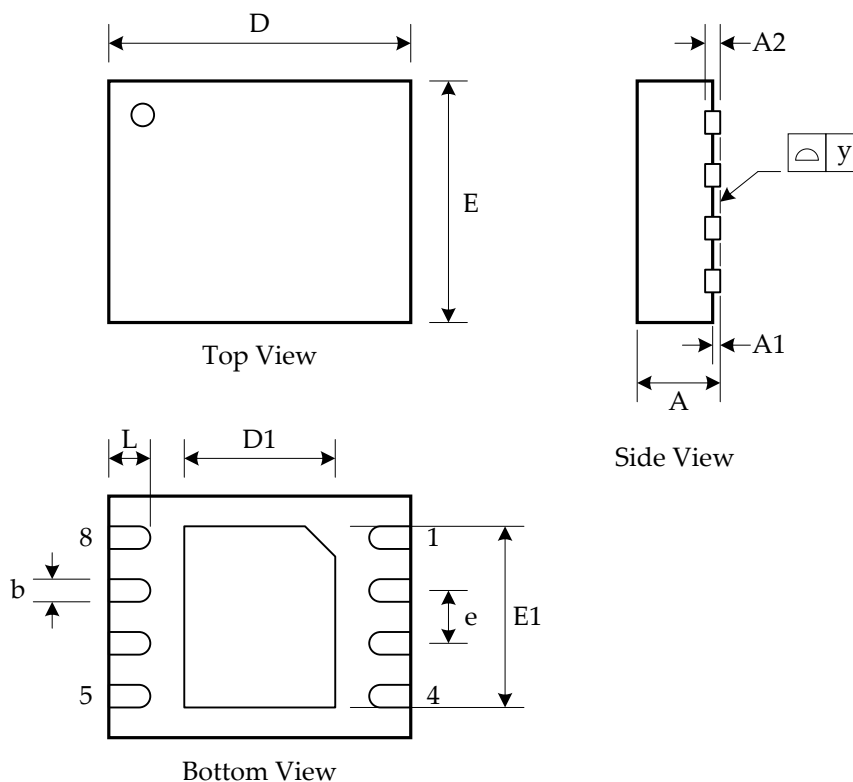
Figure 53: WSON8(6*5mm) Package

Table 25: The Package Dimensions of WSON8(6*5mm)

Symbol Unit		A	A1	A2	b	D	D1	E	E1	e	y	L
mm	MIN.	0.70		0.19	0.35	5.90	3.25	4.90	3.85		0.00	0.50
	NOM.	0.75		0.22	0.42	6.00	3.37	5.00	3.97	1.27 BSC	0.04	0.60
	MAX.	0.80	0.05	0.25	0.48	6.10	3.50	5.10	4.10		0.08	0.75
Inch	MIN.	0.028		0.007	0.014	0.232	0.128	0.193	0.151		0.000	0.020
	NOM.	0.030		0.009	0.016	0.236	0.133	0.197	0.156	0.050 BSC	0.001	0.024
	MAX.	0.032	0.002	0.010	0.019	0.240	0.138	0.201	0.161		0.003	0.030

Notes:

1. Package length and width do not include mold flash.

2. The exposed metal pad on the bottom of the package is connected to device ground (GND pin), so that it can either connect to GND or be left floating.
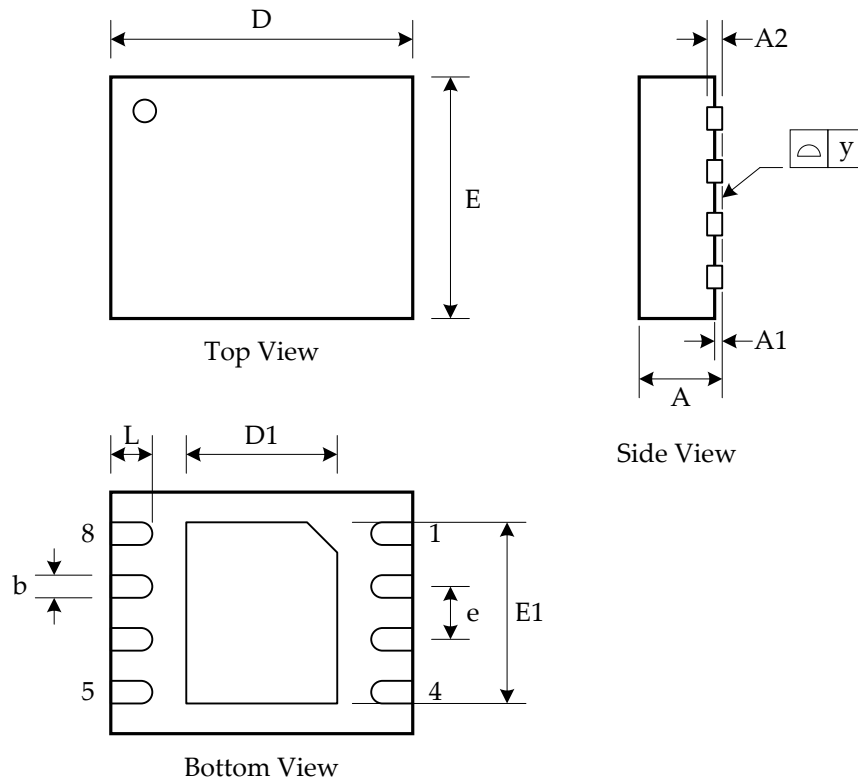
11.4. WSON8 (8*6mm)

Figure 54: WSON8(8*6mm) Package

Table 26: The Package Dimensions of WSON8(8*6mm)

Symbol / Unit		A	A1	A2	b	D	D1	E	E1	e	y	L
mm	MIN.	0.70			0.35	7.90	3.25	5.90	4.15		0.00	0.55
	NOM.	0.75		0.20	0.40	8.00	3.42	6.00	4.22	1.27	0.04	0.60
	MAX.	0.80	0.05		0.45	8.10	3.50	6.10	4.40		0.08	0.65
Inch	MIN.	0.028			0.014	0.311	0.128	0.232	0.163		0.000	0.022
	NOM.	0.030		0.008	0.016	0.315	0.135	0.236	0.166	0.050	0.001	0.024
	MAX.	0.032	0.002		0.019	0.319	0.138	0.240	0.173		0.003	0.027

Notes:

1. Package length and width do not include mold flash.
2. The exposed metal pad on the bottom of the package is connected to device ground (GND pin), so that it can either connect to GND or be left floating.

11.5. TFBGA-24(6*4 ball array)
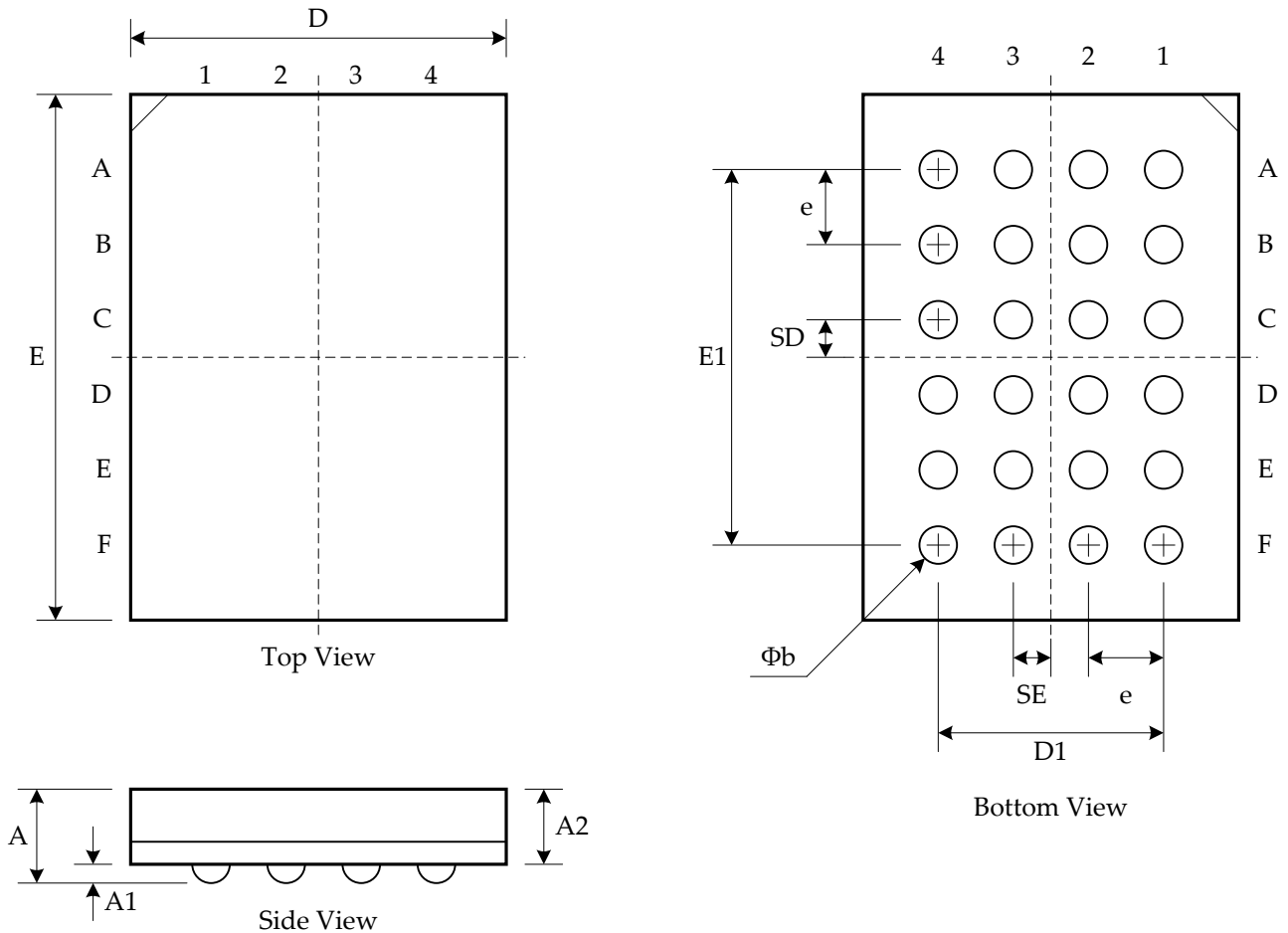
Figure 55: TFBGA-24(6*4 ball array) Package

Table 27: The Package Dimensions of TFBGA-24(6*4 ball array)

Symbol Unit		A	A1	A2	b	D	D1	E	E1	e	SE	SD
mm	MIN.		0.25		0.35	5.95	3.00 BSC	7.95	5.00 BSC	1.00 BSC	0.50 TYP	0.50 TYP
	NOM.		0.30	0.85	0.40	6.00		8.00				
	MAX.	1.20	0.35		0.45	6.05		8.05				
Inch	MIN.		0.010		0.014	0.234	0.118 BSC	0.313	0.197 BSC	0.039 BSC	0.020 TYP	0.020 TYP
	NOM.		0.012	0.033	0.016	0.236		0.315				
	MAX.	0.047	0.014		0.018	0.238		0.317				

Notes:

Package length and width do not include mold flash.

11.6. SOP16 (300mil)
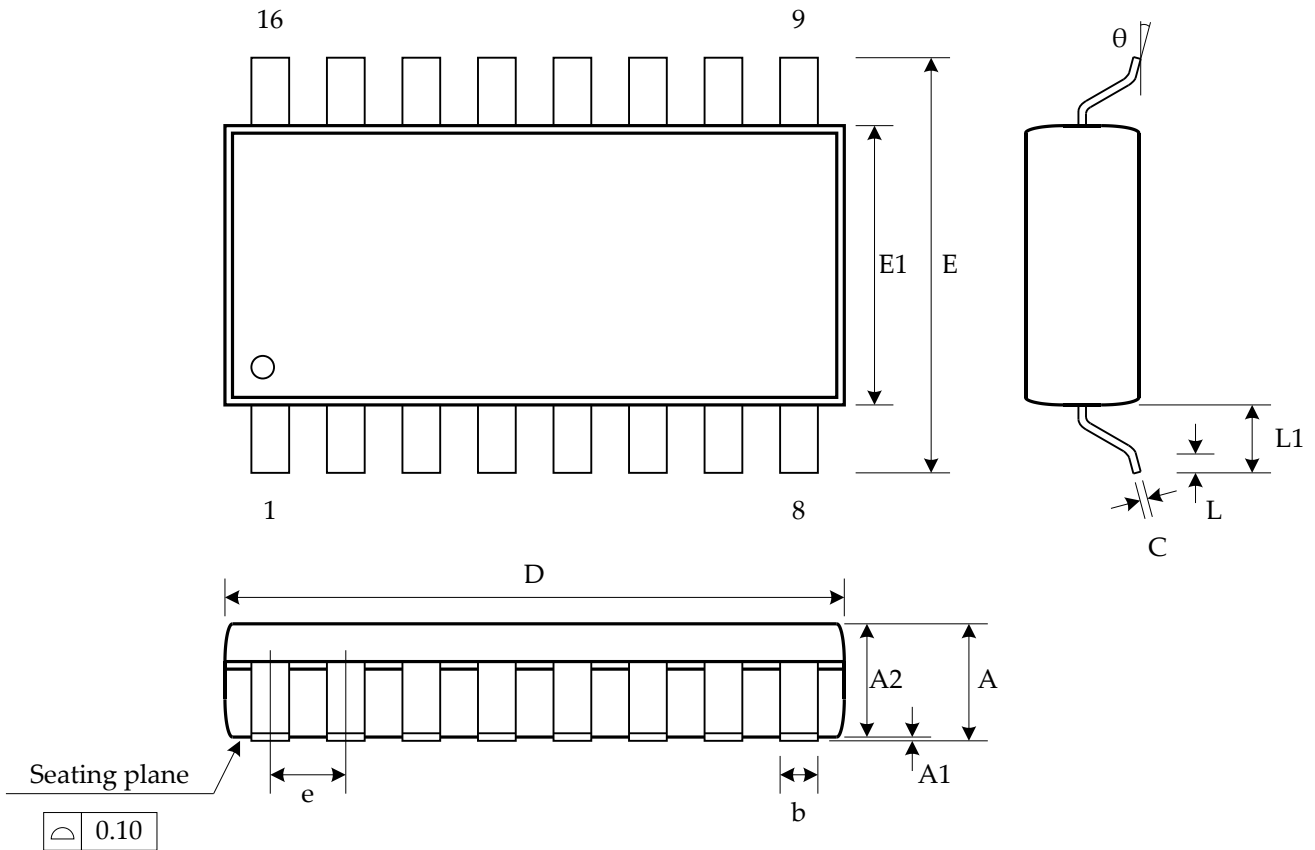
Figure 56: SOP16(300mil) Package

Table 28: The Package Dimensions of SOP16(300mil)

Symbol		A	A1	A2	b	C	D	E	E1	e	L	L1	θ
Unit													
mm	MIN.	2.36	0.10	2.24	0.36	0.20	10.10	10.10	7.42		0.40	1.31	0
	NOM.	2.55	0.20	2.34	0.41	0.25	10.30	10.35	7.52	1.27 BSC	0.84	1.44	5
	MAX.	2.75	0.30	2.44	0.51	0.30	10.50	10.60	7.60		1.27	1.57	8
Inch	MIN.	0.093	0.004	0.088	0.014	0.008	0.397	0.397	0.292		0.016	0.052	0
	NOM.	0.100	0.008	0.092	0.016	0.010	0.405	0.407	0.296	0.050 BSC	0.033	0.057	5
	MAX.	0.108	0.012	0.096	0.020	0.012	0.413	0.417	0.299		0.050	0.062	8

Notes:

1. Package length and width do not include mold flash.

2. Seating plane: Max. 0.10mm.

11.7. USON8 (4*4mm)
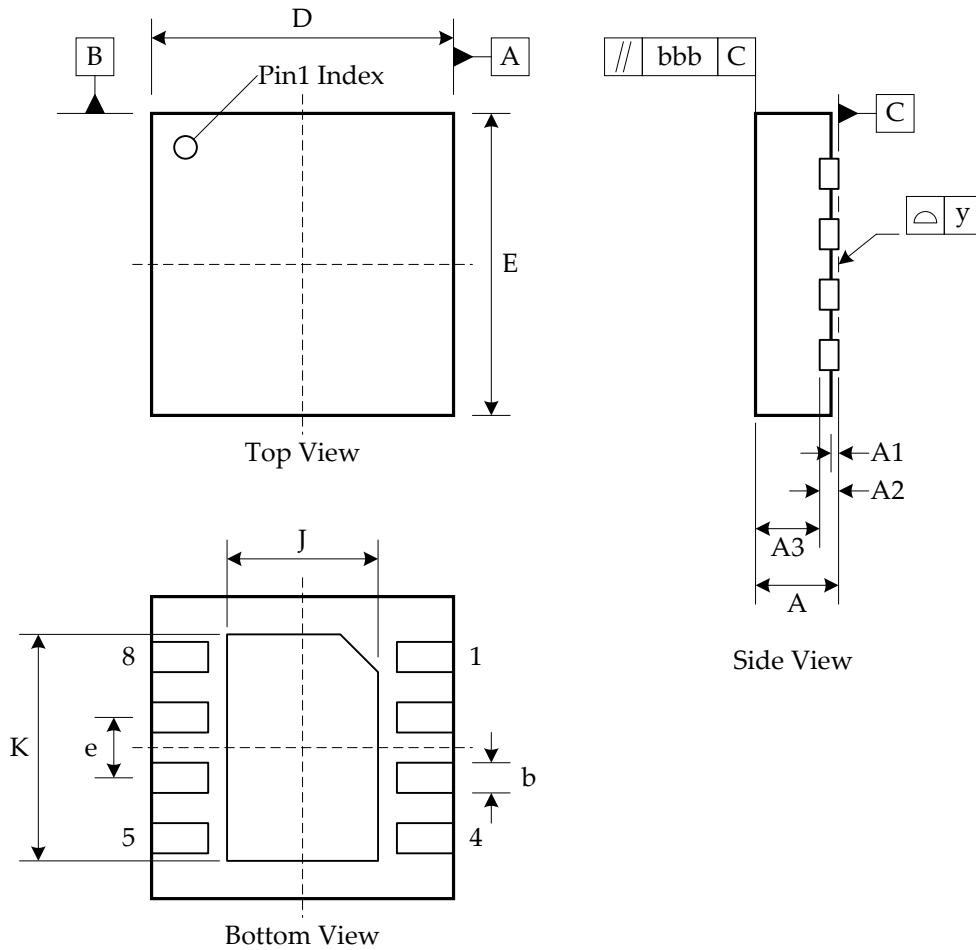
Figure 57: USON8(4*4mm) Package

Table 29: The Package Dimensions of USON8(4*4mm)

Symbol Unit		A	A1	A2	A3	b	D	E	e	J	K	L
mm	MIN.	0.40	0.00	0.15 REF	0.25	0.25	3.90	3.90	0.8 BSC	2.20	2.90	0.35
	NOM.	0.45	---		0.30	0.30	4.00	4.00		2.30	3.00	0.40
	MAX.	0.50	0.05		0.35	0.35	4.10	4.10		2.40	3.10	0.45
Inch	MIN.	0.015	0.000	0.15 REF	0.009	0.009	0.153	0.153	0.8 BSC	0.086	0.114	0.013
	NOM.	0.017	---		0.011	0.011	0.157	0.157		0.090	0.118	0.015
	MAX.	0.019	0.001		0.013	0.013	0.161	0.161		0.094	0.122	0.017

Notes:

1. Package length and width do not include mold flash.
2. The exposed metal pad on the bottom of the package is connected to device ground (GND pin), so that it can either connect to GND or be left floating.

11.8. SOP8 (150mil)
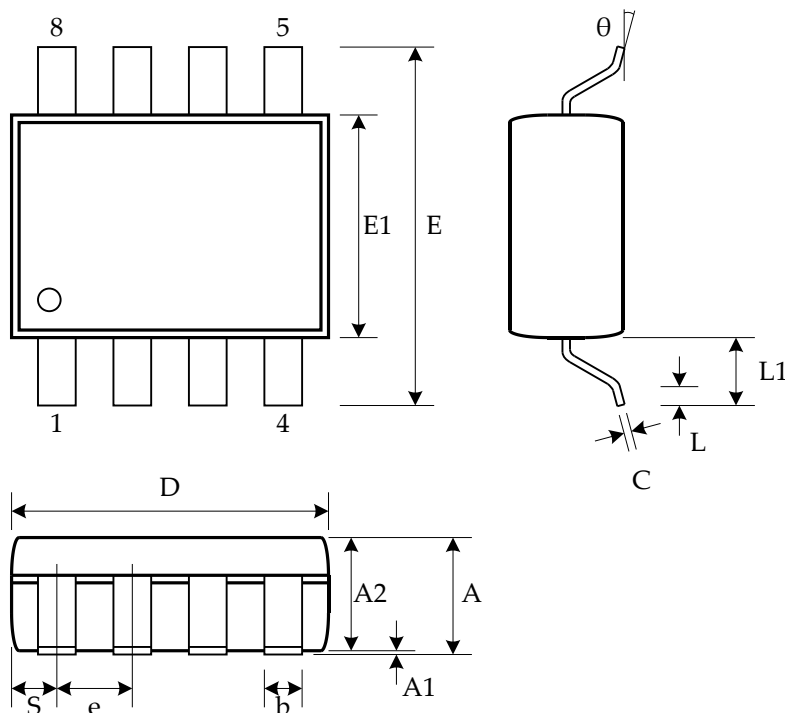
Figure 58: SOP8(150mil) Package

Table 30: The Package Dimensions of SOP8(150mil)

Symbol Unit		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	MIN.	--	0.10	1.35	0.36	0.15	4.77	5.80	3.80	--	0.46	0.85	0.41	0
mm	NOM.	--	0.15	1.45	0.41	0.20	4.90	5.99	3.90	1.27	0.66	1.05	0.54	5
mm	MAX.	1.75	0.20	1.55	0.51	0.25	5.03	6.20	4.00	--	0.86	1.25	0.67	8
Inch	MIN.	--	0.004	0.053	0.014	0.006	0.188	0.228	0.150	--	0.018	0.033	0.016	0
Inch	NOM.	--	0.006	0.057	0.016	0.008	0.193	0.236	0.154	0.05	0.026	0.041	0.021	5
Inch	MAX.	0.069	0.008	0.061	0.020	0.010	0.198	0.244	0.158	--	0.034	0.049	0.026	8

Notes:

Package length and width do not include mold flash.

11.9. USON8 (4*3mm)

Top View　　　　　　　　　　Side View

Bottom View
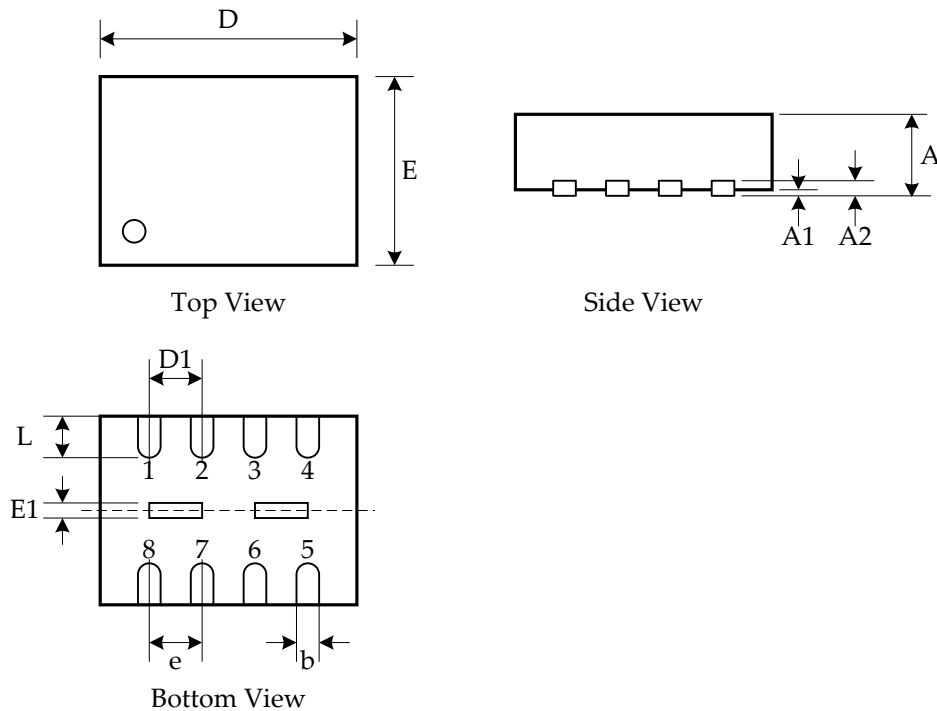
Figure 59: USON8(4*3mm) Package

Table 31: The Package Dimensions of USON8(4*3mm)

Symbol Unit		A	A1	A2	b	D	D1	E	E1	e	L
mm	MIN.	0.50	0.00	00	0.25	3.90	0.70	2.90	0.10	0.80 BSC	0.55
	NOM.	0.55	0.02	0.15	0.30	4.00	0.80	3.00	0.20		0.60
	MAX.	0.60	0.05	00	0.35	4.10	0.90	3.10	0.30		0.65
Inch	MIN.	0.020	0.000	00	0.010	0.153	0.027	0.114	0.004	0.31 BSC	0.022
	NOM.	0.022	0.001	0.006	0.012	0.157	0.031	0.118	0.008		0.024
	MAX.	0.024	0.002	00	0.014	0.161	0.035	0.122	0.012		0.026

Notes:

1. Package length and width do not include mold flash.
2. The exposed metal pad on the bottom of the package is connected to device ground (GND pin), so that it can either connect to GND or be left floating.

12. Revision History

The table below shows the revision history of this document.

Date	Version	Revision
Nov 18, 2020	v1.0	NeuMem initial release.

13. Important Notice

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